

Performance and Design Evaluation of Switch-Mode Power Supplies - AC Interface Issues

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EXECUTIVE SUMMARY

The overall objective of this effort is to influence manufacturers to build, and end-users to buy equipment employing more energy-efficient and more power quality-compatible power supplies. These enhanced supplies will play an important roll in success of the future "all electronic" office. In order to do this, an understanding of the technical and economic drivers in the office equipment manufacturer's selection of power supply technology is required. This understanding will come from baseline performance testing and analysis of both past and present power supply designs. Later, incentives and better alternatives for enhanced power supplies need to be identified and developed. Ultimately, partnering with the major suppliers and selected end-users is likely to be necessary to bring about any significant change in power supply performance.

The first step, and the specific objective of this project is to assess the state of current power supply technology and to begin to understand the technical and economic drivers in the office equipment manufacturer's selection of power supply technology.

PC and small workstation power supplies in the range of 100W - 600W, removed from their associated PC systems were selected for test from three categories:

1. Older power supply technology units from name brand PCs such as the classic XT, and AT systems. These model units were labeled AA-FF in our tests.
2. Current power supply technology units as are now used in 486 and the Pentium PC systems. These model units were labeled A, C, D, E, and F in our tests.
3. Specialty and prototype power supply technology such as "energy-star" labeled, enhanced ride-through, high-efficiency, power factor-corrected or 3-Volt logic supplies. These model units were labeled B, G, H, and GG in our tests.

The test procedure is based on the SC-450 test protocol. Three system compatibility concerns and their related tests are as follows.

1. Energy Performance
SC-450 Test EP1-- Operating Efficiency
2. Impact on Power Source
SC-450 Test E1 -- Current Harmonic Generation
3. Immunity to Power Source
SC-450 Test I1 -- Under-Voltage Response
SC-450 Test I2 -- Over-Voltage Response
SC-450 Test I3 -- Voltage Sag Response
SC-450 Test I4 -- Voltage Swell Response
SC-450 Test I7 -- 500 Hz Ring-Wave Surge Response
SC-450 Test I7 -- Switching Surge Response
SC-450 Test I9 -- 1.2/50 μ s-8/20 μ s Combination-Wave Surge Response

SC-450 Test I10 -- Electrical Fast Transient (EFT) Burst-Wave Surge Response
 Findings and suggestions are summarized below.

1. Findings From Efficiency Evaluation

- Two major circuit topologies are most often used: (a) Half-Bridge Converter and (2) Forward Converter with RCD Clamp
- No evidence showing which circuit topology is more efficient
- Measurable lossy components are: (1) device conduction, (2) device switching, (3) output diode voltage drop, (4) magnetic components, (5) clamping and snubbing components, (6) input rectifier, (7) cooling fan, and others.
- Major efficiency improvements may be obtained by:
 - a. Using better devices that would reduce the turn-on resistance of the high voltage power MOSFET and the voltage drop of the Schottky diode.
 - b. Using advanced circuit topologies such as the soft-switching active clamp circuit to replace the lossy RCD clamp circuit. For a boost converter with power factor correction circuit, the soft-switching technique should also be used to improve the efficiency.
- Figure E-1 compares the test results of the power supply efficiency profiles for 25%, 50%, and 100% loads at the rated input voltage. In general, power supplies with new designs are more efficient than old designs, possibly due to availability of better devices.

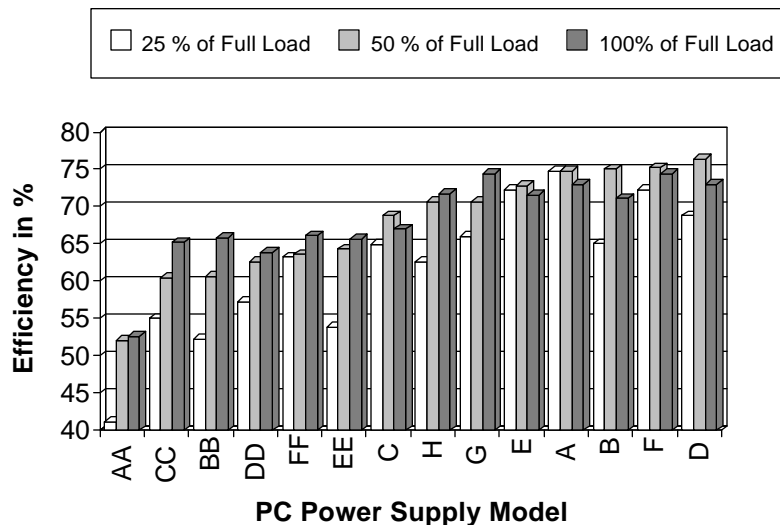


Figure E-1
 Power Supply Efficiency Profile for 25%, 50%, and 100% Loads at 100% of Nominal Input Voltage

2. Findings from Harmonics Evaluation

- Figure E-2 compares the harmonic performance of the tested power supplies with IEC555-2.
- Without adding a front-end boost converter with power factor correction, all PC power supplies failed to pass the IEC555-2 Standard.
- All three models equipped with a front-end boost converter show superior performance in harmonic elimination.
- The remaining PC power supplies were not equipped with the boost converter power factor correction circuit, possibly due to cost constraint.
- No significant harmonic performance difference between old and new power supply models unless a boost converter circuit is used.

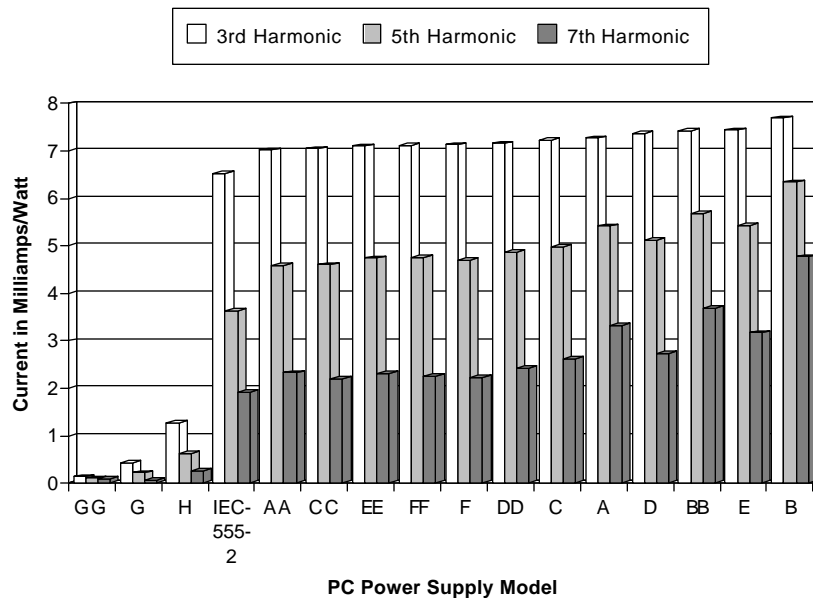


Figure E-2
PC Power Supply Harmonic Current Distortion Per Harmonic

3. Findings from Under-Voltage and Voltage Sag Tests

- Ride-through performance not only relies on the dc link bulk capacitor, but also the transformer turns ratio and the method of supplying voltage to the PWM IC.
- All tested power supplies performed better than the CBEMA curve for under-voltage ride-through.
- Most of the tested power supplies can operate below 80% of the nominal voltage at steady-state with 100% of full load.

- Figure E-3 compares the minimum steady-state operating voltage at the full load condition.
- Figure E-4 compares the under-voltage ride-through of three power supply models with the CBEMA curve. Model DD represents the old design, Model A represents the new design, and Model G is the design with a front-end boost converter for harmonic control.
- There is no significant difference between the old and the new PC power supply designs in under-voltage ride-through, but the new design with a front-end boost converter has better ride-through capability even though they tend to use smaller dc link capacitors.
- An under-voltage operation could fail the input diode bridge and blow the fuse if these are not sized for the increased current.

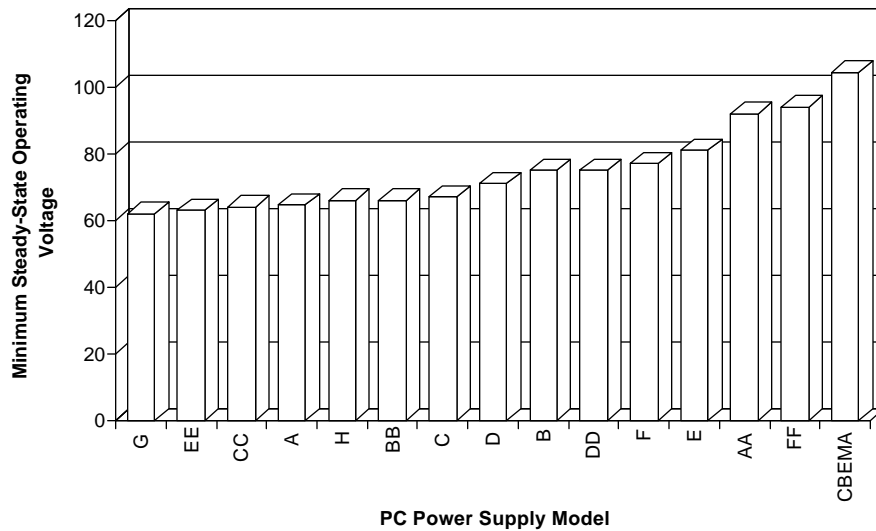


Figure E-3
Minimum Steady-State Operating Voltage at 100% of Full Load

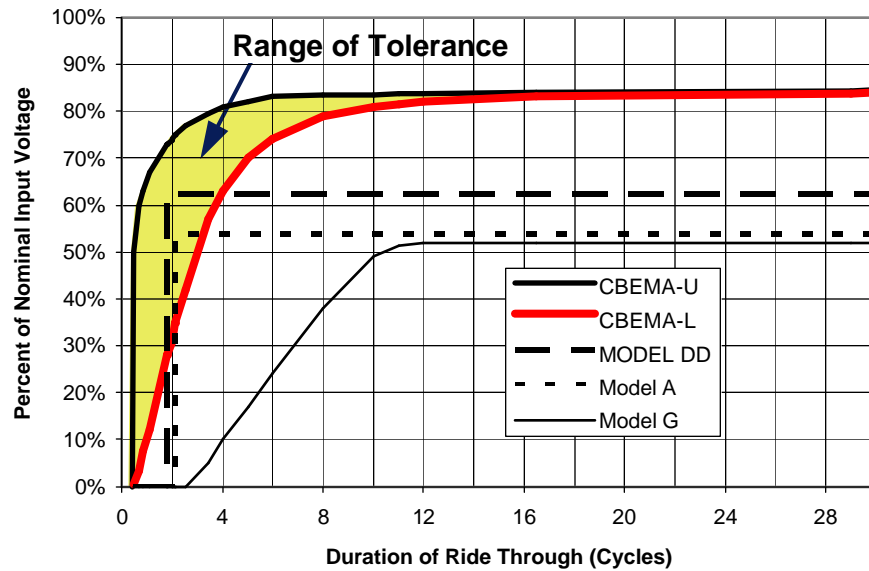


Figure E-4
Voltage-Tolerance Test Results Compared to CBEMA Curve

4. Test Summary Comparison with the SC-450 Protocol

Table E-1 is a summary of the actual tests results as compared to the System Compatibility Protocol Document, SC-450.

Table E-1, Test Summary

Did the Device Meet Expectations of the Proposed Criteria of the SC-450 document?													
Model	Test B1	Test EP1	Test EI	Test I1	Test I2'/I4	Test I3	Test I4	Test I5	Test I7	Test I9	Test I10	Test I11	Test I12
Current Technology Power Supplies													
A	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
C	Y	3	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
D	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
E	Y	Y	Y	2	Y	Y	Y	Y	Y	4	4	Y	Y
F	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
"Special" Advanced Technology Power Supplies (Power Factor Correction, Energy Star)													
B	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
G	Y	Y	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	Y
H	Y	Y	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	Y
GG	Y	4	Y	4	4	4	4	Y	4	4	4	4	4
Older Technology Power Supplies													
AA	Y	1	Y	Y	4	Y	Y	Y	4	4	4	4	4
BB	Y	3	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	Y
CC	Y	3	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	Y
DD	Y	3	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	Y
EE	Y	3	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	Y
FF	Y	3	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	Y

Notes:

- 1). Exhibited lowest efficiency of all units tested. Efficiency did not exceed 55% at any load.
- 2). Unit passed test criteria per the CBEMA curve. However, the power supply was eventually damaged during the low voltage test. Although the unit failed outside of the manufacturer's voltage range specification, the manufacturer redesigned product based on the PEAC test results. All current PCs are being shipped with the improved power supply.
- 3). Efficiency was lower than expected.
- 4). Not Tested.

5. Suggestions for Future Work

- Test the power supplies with their actual loads such as a computer or an office machine.
- Test the premise or a commercial building power system energy cost instead of individual power supplies.
- Technology developments are required for better and cheaper power supply ac interfaces to comply with upcoming power quality standards.
- Advanced power electronics technologies are available but need to be implemented for justification of cost and performance, especially to meet the trend of the computer industry in low-voltage logic design. Examples of these technologies are soft-switching boost converters, active-clamp forward converters, and synchronous rectifiers.

INTRODUCTION

1.1

Background

The personal computer (PC) is the most versatile piece of equipment in the modern office, workplace, and home. Almost daily we find new uses for this indispensable appliance, and as we look toward the future, we will undoubtedly find ever-expanding roles for PCs in all sectors. Because of its versatility, increasing numbers of PCs are being connected to the power system, peripheral equipment, and each other. As PCs become more indispensable at work and home, and as offices consume more energy, utilities and their customers are becoming more concerned about performance of the PC as a load. The generation of harmonic currents and PC sensitivity to voltage sags, surges, and other power quality-related events are among the system compatibility issues that must be resolved. Available data is insufficient to fully characterize the power quality and system compatibility performance of PCs, but does indicate a very wide range of performance. At the same time, efforts to reduce the size and cost of PC power supplies may further complicate PC compatibility. In the past, PC users have relied on expensive add-on filters, uninterruptible power supplies, and transient voltage surge suppressors to reduce harmonic emissions and enhance PC immunity. A more efficient and economical approach may be to encourage PC manufacturers to design compatibility into their products to avoid these costly add-ons and potential disruption of customer operations.

1.2

Project Description

Power supplies for personal computers are rarely built by the original equipment manufacturers. Today's PC power supplies are nearly all furnished by third party manufacturers according to the PC Original Equipment Manufacturer (OEM) specifications. The same power supply model is not always used in all computers having the same model number. Some of the older power supplies to be tested are designed and manufactured by the OEM or computer name brand manufacturer. Given these factors, supplies will be selected to provide a representative sample of the most commonly used power supplies in the largest selling PC units.

- 1. Older power supply samples (not of current manufacturer):** were obtained and tested from a stock of outdated computer units on hand. Only informal manufacturer involvement will be solicited to identify type, rating, or source of power supplies as is required.

- 2. Current manufacturer power supply samples:** involve a formal agreement with the specifier or PC manufacturer. The PC manufacturers providing power supplies that are commonly used in their computers will be asked to:
 - Sign an agreement allowing testing of power supplies, confirming knowledge of test protocols and releasing test results to sponsoring utilities.
 - Provide general product data such as power circuit block diagrams or simplified schematics, principles of operation, and application information.
 - Furnish power supply samples, generally eight units (4 samples x 2 models for 486 or Pentium) of current manufacturer and replace any failed samples.
 - Review the results of testing performed on their products and provide comments, clarifications or suggestions as appropriate.
- 3. Specialty and prototype power supply samples:** were obtained by individual arrangements with the PC or power supply developer. Any proprietary restrictions, test limitations, will be covered in a purchase agreement or MOU as appropriate.

This project evaluated and characterized the performance of power supplies commonly used in personal computers. The power supply compatibility with the utility power system, and the ability of the power supply to maintain a regulated DC output during various input conditions (over-voltages, undervoltages, sags, swells, and surges) with loads ranging from no load to full load was analyzed. This project concentrated on establishing system compatibility test criteria; developing test procedures; characterizing the immunity, emissions, and energy performance characteristics of 50-watt to 250-watt PC power supplies removed from their associated PC systems; and encouraging manufacturer involvement and enhancement of PC power supply compatibility.

1.4

Objective

The main objective of this project is to obtain a better understanding of the power quality performance of personal computer power supplies and to improve their compatibility with the utility. It is our hope that results from this task will help the utility and customers make informed purchases of PC products. The primary project goals are to:

- o Establish PC System Compatibility (SC) test criteria;
- o Develop evaluation procedures where none currently exist;
- o Characterize available PCs on the market through laboratory evaluation; and
- o Compare PC power quality performance parameters that concern both utilities and customers.

1.5

General Overview

The PC power supplies were tested in accordance with selected guidelines from the SC-450 test protocol (Draft 4, June 1994) to determine their electrical characteristics. Testing was performed at PEAC's Power Quality Testing Facility (PQTF). Table 1-1 shows which tests of the SC-450 were performed in this project.

Table 1-1
SC-450 Tests Performed on the Host Utility PC Project

Energy Performance
Test EP1. Characterization of PC Power Supply Efficiency
Emissions
Test E1. Characterization of Input Total Harmonic Distortion
Immunity
Test I3. Susceptibility to Voltage Sags and Momentary Outages
Test I4 Susceptibility to Voltage Swells
Test I5 500 Hz Ring-Wave Surge Test
Test I7.0.5 μ s-100 kHz Ring Wave Surge Test
Test I9. 1.2/50 μ s-8/20 μ s Combination-Wave Surge Test
Test I10 Electrical Fast Transient (EFT) Burst-Wave Surge Test
Test I4' Swell to Fail Tests*

* Test I4' was added in order to locate the upper portion of the voltage tolerance envelope.

Generally, two units from each model were evaluated for tests EP1 and E1 for the current and special category models. The remaining tests were conducted on a single unit of each model. If any of the tests resulted in damage, additional units of the same model were retested. If a power supply sample failed at any point in the testing, it was removed from the test chamber and replaced with an identical sample before testing resumed. If the new sample also failed the test, no more samples were subjected to the test. The results shown for each model in this report are the best case performance for all samples of that model. If significant variations in performance were noted between two samples of the same model of power supply, these results will be noted within the report. The data in this report has been arranged so that the results cannot be correlated to any particular manufacturer.

TEST DESCRIPTION

2.1

Detailed Test Plan

This project will provide detailed results of performance for a range of power supply types, fifteen different models in all. Tests are selected from PEAC's, Test Protocol for System Compatibility of Power Supplies and Peripheral Device Interface Ports used in Personal Computers, SC-450 Draft 4, June 1994. The following table identifies the key application concerns, and investigation methods selected to address these concerns.

Table 2-1
Test Plan Based on SC-450 Test Protocol

Power supply test methods, variables and conditions to address application concerns in electronic office system		
<i>Application Concerns</i>	<i>Method of Addressing</i>	<i>Variables or Conditions</i>
Energy Performance		
Operating Efficiency	SC-450 Test EP1,I12	Vrms, Vthd, Zline, % load
Input Power Factor	SC-450 Test EP1,I12	Vrms, Vthd, Zline, % load
Impact on Power Source		
Current Harmonic Generation	SC-450 Test E1, I12	Vrms, Vthd, Zline, % load
Filtering Load Factor	SC-450 Test B-1 new	10Hz - 10MHz, L-N & L-G
Immunity to Power Source		
Response to Low Line Voltage	SC-450 Test I1	87% V & Vtrip, load varies
Response to High Line Voltage	SC-450 Test I2	Vrms = 106%, load varies
Susceptibility to Voltage Sags	SC-450 Test I3	.25 Sec, 3 levels, 2 loads
Susceptibility to Voltage Swells	SC-450 Test I4	.25 Sec, V=150, 2 loads
Response to Capacitor Switching	SC-450 Test I5	@ 25% load, 2 pu
Response to Switching Surge	SC-450 Test I7	@ 25% load, 1 & 3
Response to Noise Burst	SC-450 Test I10	@ 25% load, 1 & 4 kV
Response to Lightning Surge	SC-450 Test I9	@ 25% load, 1.5kA, 3kV
High Line Voltage Failure Mode	new test	@ 50% load, 2pu

Lab data sheets have been developed to guide the testing. Data sheets #1 and #2 show the sequence of tests, the specific data to be collected and the range of expected conditions for each test.

2.2

Procedures

The project was performed with the following procedures.

- Select a sample set of power supplies including older, used over the last 5-10 years, current manufacturer in common use today and future or specialty designs. For current designs attempt to obtain a written understanding with the PC manufacturer.
- Test these supplies to determine the emissions, immunity, and energy performance ranges and related trends.
- Evaluate circuits and identify design features and components that are most influential in the measured performances.
- Compare performances relative to generic designs and components.
- Encourage industry participation and coordinate with related activities
- Present summary of findings at conference
- Prepare a report on results

2.3

Test Setup

Test procedures and setup have been described in detailed in SC-450 document. Figure 2-1 illustrates the test facility for efficiency measurement. The testing facility should have the ability to display and simultaneously record signals from at least 4 channels in order to monitor single-phase voltages and currents at the input and output of the device under test, as seen in Fig. 2-1. Regardless of the method used in data acquisition, instruments should be selected with an accuracy of $\pm 1\%$ of full scale or better. Word size of any microprocessor used in data acquisition should be sufficient to maintain this accuracy.

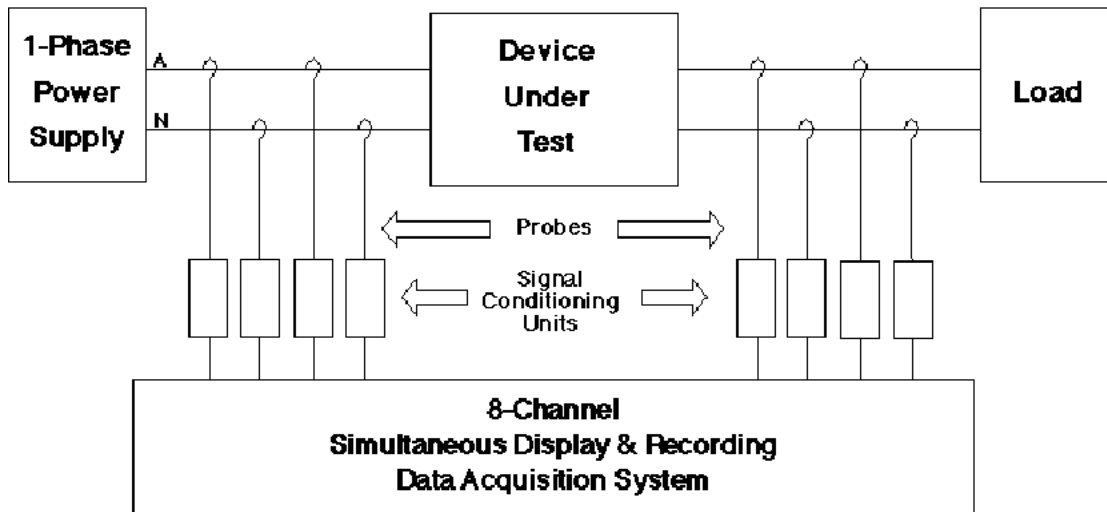
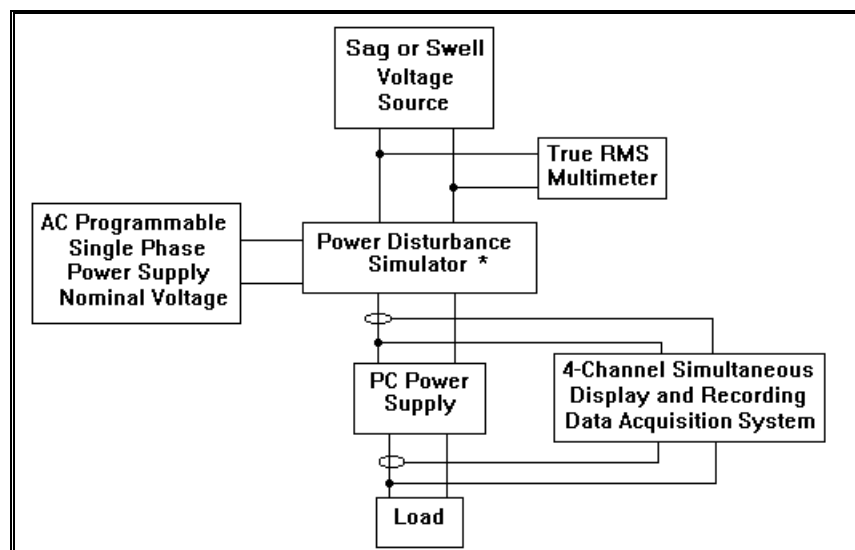


Figure 2-1
Simultaneous measuring of input and output power.

Figure 2-2 illustrates the test setup for voltage sag or swell test. The sag or swell voltage is added on top of the programmable nominal voltage. The input and output voltage and current of the power supply are monitored simultaneously with the data acquisition system similar to or the same as that used in efficiency measurement.



*Capable of switching between nominal voltage source and sag or swell voltage source for selected time durations.

Figure 2-2
Voltage Sag and Swell Test Setup

Figure 2-3 shows the surge testing setup. The most important consideration in this setup is the differential measurement. Because the voltage level is much higher than the premise, the test equipment and measurement instrument must be properly grounded to ensure safety and accurate measurement.

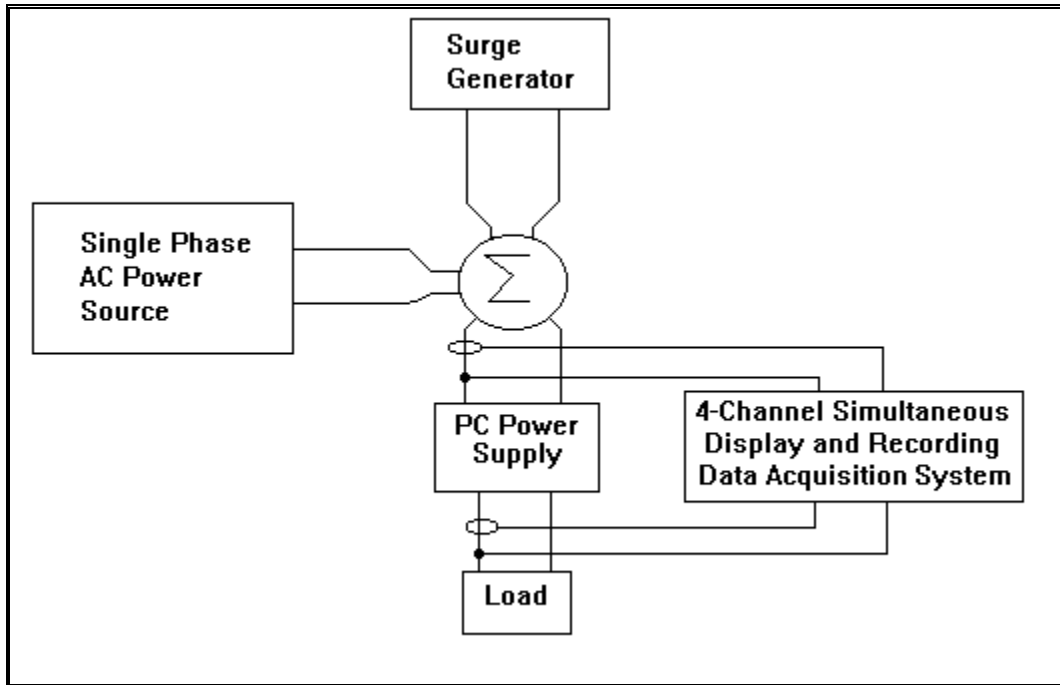


Figure 2-3
Surge Testing Setup

TEST RESULTS AND ANALYSIS

3.1

Fundamentals of a PC Power Supply

3.1.1

Harmonic Sources

The cause of the harmonics in a computer power supply is mainly due to the rectifier-capacitor charging. Figure 3-1 is the basic building block of a PC power supply. The ac input line draws current only when the input voltage is higher than the rectifier dc output voltage which is typically smoothed by a bulky capacitor. Because the capacitor impedance is approximately zero, the current charged through rectifier is only limited by the source impedance and the rectifier voltage drop. As a result, the charging current presents a spiky waveshape with a full spectrum of harmonics. This is a common problem in all the traditional PC power supplies. Without a dramatic design change of the power supply front-end circuit, all the traditional power supplies will face the same harmonic distorted input current problems.

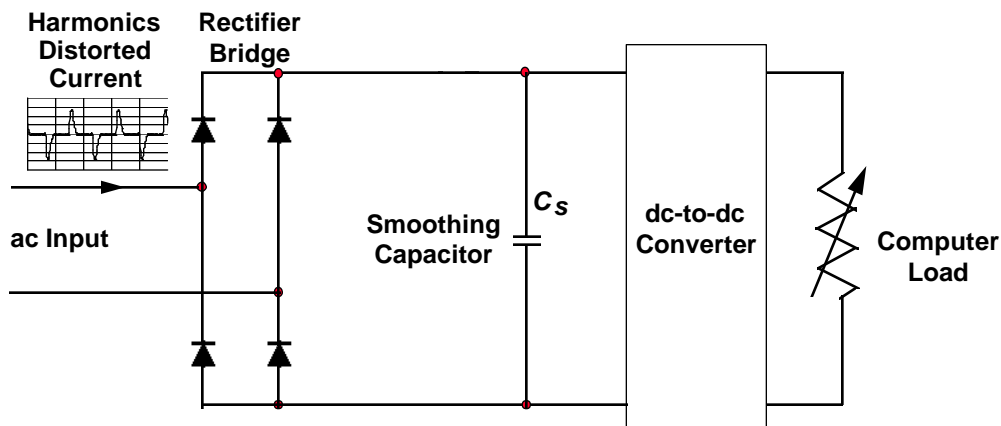


Figure 3-1
Basic Structure of a PC Power Supply

Up to this time, the most well-known cost effective approach to fix the harmonic problem is to add a front-end boost converter between the rectifier and the bulky capacitor, shown in Figure 3-2. The basic components required in a boost converter are an inductor, L_s , a switch, Q_s , a diode, D_s , and a capacitor, C_s . As a dual function to the voltage smoothing capacitor, C_s , the boost inductor, L_s , is to serve as a current smoothing element. Turning on the transistor, Q_s , will store the energy in the inductor, while turning off the transistor will divert the inductor energy to the voltage smoothing capacitor, C_s . By employing a feedback control loop, the inductor current will always track the positive half sine wave

with the condition that the voltage across, C_s , must be higher than the peak input ac voltage. The resulting input ac current will be a distortion-free sine wave.

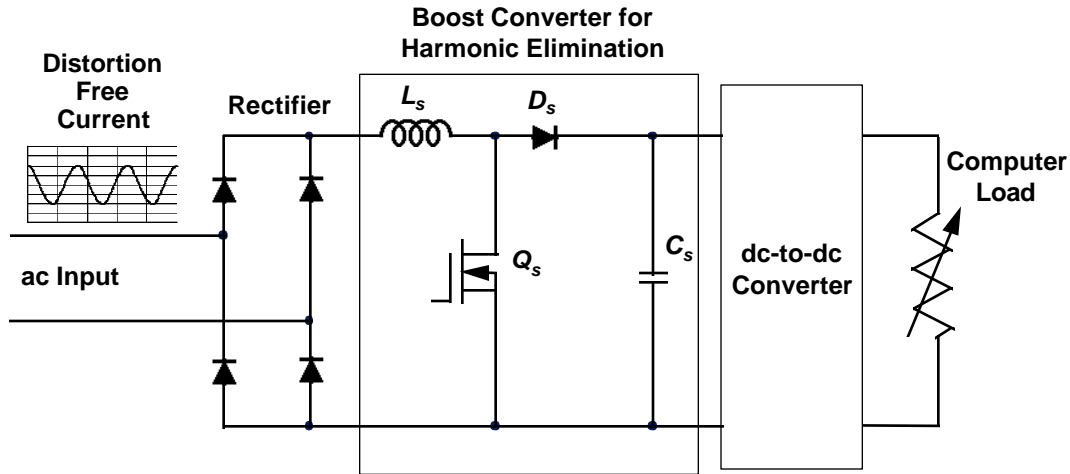


Figure 3-2

Adding a Harmonic Elimination “Boost Converter” into an Ordinary PC power supply

3.1.2

Ride Through Capability

To increase the ride through capability of a PC power supply, one would think that adding as much storage capacitance would serve the purpose. This, however, is only partially true. Consider the block diagram of a dc-to-dc converter, shown in Figure 3-3. The output voltage, typically for +5V, is regulated by pulse-width-modulation (PWM) control, and the high voltage to low voltage conversion is isolated by a transformer with a certain turns ratio. If there is a voltage sag or momentary outage, the voltage across the smoothing capacitor will be dropping with a rate that is determined by the capacitance and the load condition. The output voltage, however, can still be regulated by increasing the duty cycle of the PWM control as long as the transformer secondary voltage is high enough to maintain +5V and +12V. If the design is to have a high transformer turns ratio, then the PWM duty cycle will be low at the normal voltage operation. When the input voltage drops during voltage sag or momentary outage, the PWM duty cycle will be increased to compensate the voltage drop until the supply voltage of the PWM control IC is lower than its designated threshold voltage (typically 9V).

According to the above description, the critical components that affect the ride through capability include: the transformer turns ratio, the PWM IC undervoltage shutdown level, the dc link capacitor, the bypass capacitor of the control IC, and the capacitors across +5V and +12V outputs. Increasing the transformer turns ratio is a way to improve the ride through capability, but the cost involved with a larger transformer could prevent manufacturers from doing this.

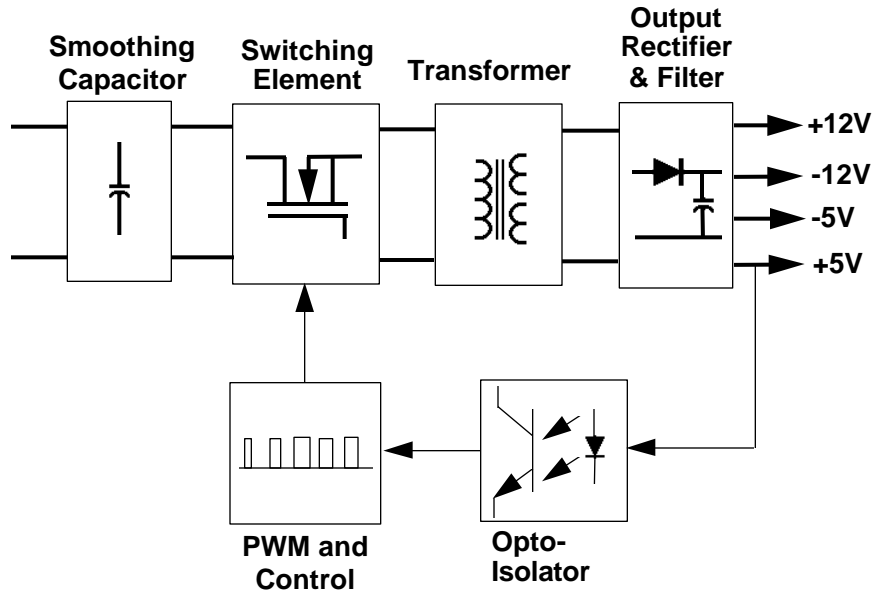


Figure 3-3
Block Diagram of a dc-to-dc Converter for a PC Power Supply

3.1.3 Efficiency Consideration

The efficiency of a PC power supply depends mainly on the lossy components in different dc-to-dc converter circuits. Among all the power supplies we tested, there are two major dc-to-dc converter circuit topologies: (1) half-bridge converter and (2) forward converter with RCD clamp, shown in Figures 3-4 and 3-5, respectively.

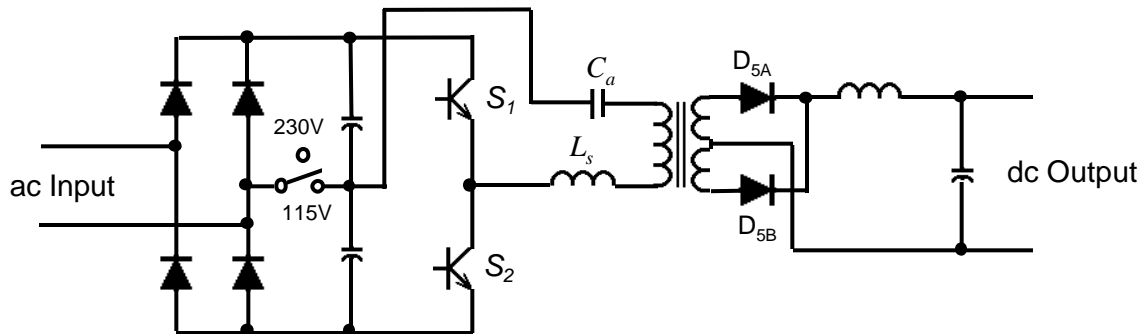


Figure 3-4
A Half-Bridge dc-to-dc Converter

A half-bridge converter normally uses the bipolar junction transistor as the switching device which is a slow switching device consuming high switching loss but low conduction loss. In our tested machines, the half-bridge converter based power supplies are typically switching less than 45 kHz but higher than 20 kHz to avoid acoustic noises.

The forward converter requires only one switching device and is potentially lower in cost than the half-bridge converter. Because the gate drive does not require isolation, this type of circuit typically uses power MOSFET as the switching device so that the gate can be directly connected to the switching regulator IC. Because the power MOSFET has less switching loss, this type of power supply is normally switching at a frequency 40 kHz or above. The problem of using power MOSFET is high conduction losses associated with the high voltage devices. The forward converter has a major drawback that a high voltage stress during device turn-off. To reduce the voltage stress, the traditional design is to add an RCD clamp circuit across the transformer primary winding. Both the conduction loss associated with the high voltage power MOSFET and the lossy clamping circuit can make this type of circuit less efficient.

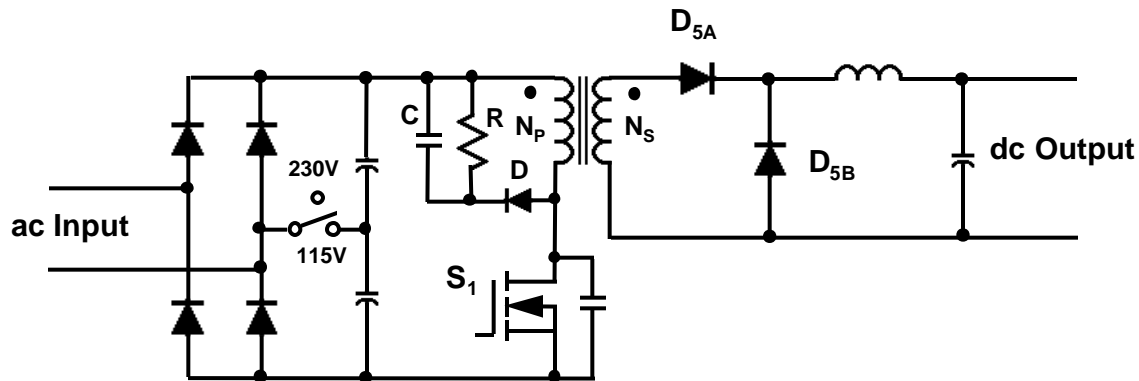


Figure 3-5
A Forward Converter with R-C-D Clamp.

There is no evidence to justify which topology is more efficient. The components used may have more impact than the circuit topology itself. However, for either type of the converter circuit used, some measurable lossy components are: (1) device conduction, (2) device switching, (3) output diode voltage drop, (4) magnetic components, (5) clamping and snubbing components, (6) input rectifier, (7) cooling fan, and others. The first three are perhaps the most critical components that affect the power supply efficiency.

Adding the front-end boost converter for harmonic elimination would definitely reduce the entire system efficiency because of the additional conduction and switching losses. It is difficult to improve the power factor while maintaining a good efficiency. The only way, to our knowledge, is to apply soft-switching techniques to eliminate the switching losses. If the forward converter is to be used for dc-to-dc power conversion, the efficiency can be improved by using active clamp circuit to replace the passive RCD clamp. The active clamp circuit reduces the voltage stress so that lower voltage power MOSFET can be used to reduce the conduction loss. The main device along with the active clamp device can both switch at the lossless condition. Different circuit topologies are shown in Appendices.

3.2

Units Tested

The PC power supplies tested were divided into three categories as defined below:

- **Old.** These power supplies are older technology units from PEAC's own computer inventory. These units were tested in order to characterize performance improvement trends. We were able to obtain six different models of "older" technology power supplies for testing..
- **Current.** These units are current technology Power Supplies that were requested from and submitted by the participating manufacturers. In this category, a total of twenty power supply samples from five different models of current technology power supplies were submitted by the manufacturer for testing.
- **Special.** These units have advanced features such as power factor correction or energy efficient Energy Star circuitry and were either taken from our own inventory or submitted by the participating manufacturers. Ten units representing four power supply models were submitted for testing in this category.

Each participating manufacturer was asked to submit two to three samples of two of their most popular power supply models. A total of thirty-six power supply samples representing fifteen different power supply models were available for characterization.

3.3

Test Results and Analysis

Test EP1. Characterization of PC Power Supply Efficiency

Overview of Test. PC's are part of an increasing percent of the total electrical energy consumption in commercial and residential applications. Today's PC's efficiency can range from 65% to 80% with potential for significantly higher efficiency in the future. The load of PCs will vary due to the end-user selection of options. It is therefore important to see how the load change will affect the PC power supply efficiency.

Discussion of Results

A. Effects of the Supply Voltage and Load Variation

Figure 3-6 below displays a PC efficiency profile for Model E at various loads and at three different input voltages. This profile is typical of what is expected from a PC power supply. As can be seen by the curves, efficiency typically improves as the power supply load is increased from 25% to 50%, tends to stabilize from 50% to 75%, and drops off as the power supply load approaches the total capacity of the unit. This trend was found to be true in most power supplies tested. However, the amount of efficiency decrease from a 75% to 100% load was found to vary.

As shown in Figure 3-6, the efficiency at the three operating voltages did not vary more than 5 % at any load for Model E. In general, the efficiency profile slightly varies with the supply voltage. This variation is due to changes of the conduction and switching losses. At low supply voltages, the device conduction duty is increased, but the switching loss is reduced. At light load conditions (<50% load), the efficiency obtained from a low supply voltage is normally better than that obtained from the rated supply voltage. In contrast, the high supply voltage favors high load conditions in terms of efficiency gains. There is not a definite number or equation to express the effect of the supply voltage to the efficiency variation because the changes of conduction and switching losses are highly nonlinear.

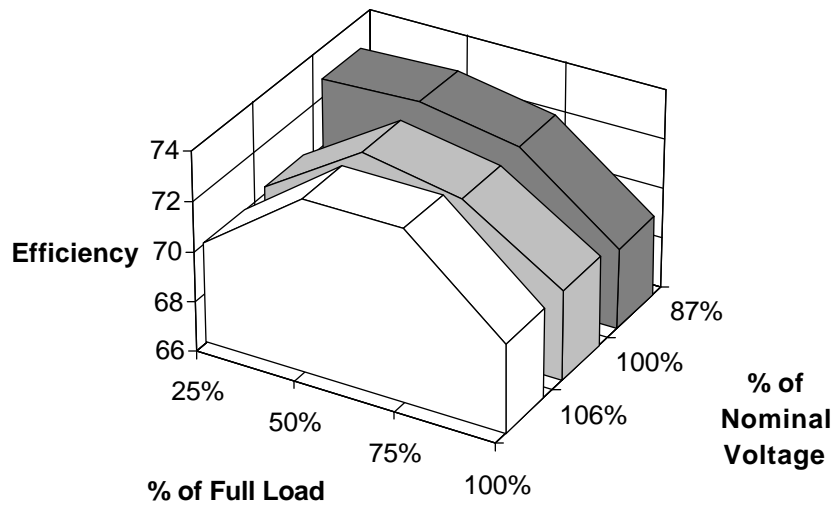


Figure 3-6
Typical PC Power Supply Efficiency Profile

B. Effects of Power Supply Design

Figure 3-7 displays the efficiency test results at 25%, 50%, and 100% loads while the power supplies were operating at 100% of nominal voltage (120 V_{ac}). In general, this figure displays the efficiency improvements from the older model power supplies to the current and advanced technology units. The efficiency improvement in the new models is mainly due to the improvement of semiconductor devices such as the switching device, Schottky diodes, and magnetic materials.

Note:

Model with best efficiency data chosen as the best case representation of the product.

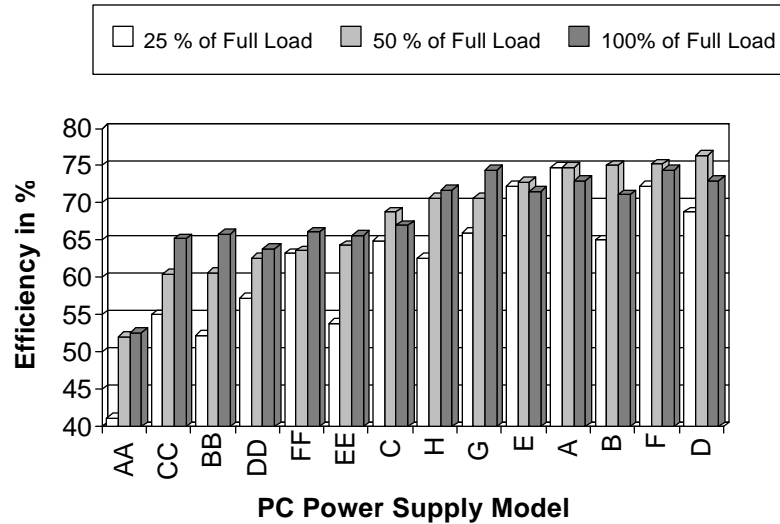


Figure 3-7

PC Efficiency Data for 25%, 50%, and 100% Loads at 100% of Nominal Input Voltage

Table 3.1 lists the circuit topology, switching frequency, and devices for different models. All the half-bridge converter type power supplies use bipolar junction transistors (BJTs) as the switching device because they have higher voltage rating and can be directly driven by the isolation transformer. None of the half-bridge converters operate at higher than 50kHz because excessive switching losses incurred in BJTs. Using the same circuit topology and the same switching device may not guarantee the same efficiency performance. Models C, D, and F all use the same half-bridge converter circuit and the same 2SC4138 BJTs, but their efficiency numbers at 50% load vary from 3.4 to 6.9 percent.

New designs tend to use power MOSFETs for high frequency operation. Model H, the work station power supply, uses the advanced resonant converters to increase the switching frequency to 2 MHz. This frequency is so far the highest switching frequency in off-the-shelf computer power supplies. The purpose of increasing switching frequency is not to improve the efficiency but to reduce the size of the power supply. It is possible to employ soft-switching techniques to improve the efficiency, but the switching frequency need not to be exceedingly high.

Table 3-1
Circuit topology, switching frequency, and devices for different models

Model	Efficiency @50% load	Circuit topology	Switching frequency	Switching device	Schocttky diode
A	74.4	Half-bridge	25kHz	2SC4242 BJTs	ERD83-04
B	71.5	Forward	42kHz	2SK1507 MOSFET	ERD83-04
C	69.5	Half-bridge	42kHz	2SC4138 BJTs	ERD83-04
D	76.4	Half-bridge	49kHz	2SC4138 BJTs	CTB-34
E	74.9	Forward	72kHz	2SA792 MOSFET	CTB-34
F	73.0	Half-bridge	48kHz	2SC4138 BJTs	CTB-34
G	71.8	Boost + Forward	93kHz 240kHz	2SK1944 MOSFET	ERD84-04
H	67.6	Boost + resonant converter	710kHz 2MHz	2SK1982 MOSFET	ERD83-04

There is additional room for improving the efficiency of buck converter type power supplies. Major efficiency improvement may be obtained from the following areas.

1. Better high voltage power MOSFETs -- The manufacturing technology is evolving to getting better higher voltage devices. The conduction voltage drop is expected to drop further with the new devices.
2. Better Schocttky diodes -- The output Schocttky diodes typically have 0.5V drop or higher, which is more than 10 percent loss of the 5V output. If the 5V output accounts for 50 percent of the loading, the conduction drop of the Schocttky diode is more than 5 percent of the total system losses.
3. Active clamp with zero voltage switching -- The resetting of the transformer magnetic field is traditionally a lossy RCD clamp. Such a clamping circuit can be lossless with the use of an auxiliary active switch. By optimizing the lossless capacitor snubber and the resonant circuit design, the switching loss can be dramatically reduced.

Test E1. Characterization of Input Current Total Harmonic Distortion (I_{thd})

Overview of Test. PC's draw non-sinusoidal ac current, creating harmonic currents in the ac power system that can interfere with communications, distribution transformers and other equipment. It is important to characterize the extent to which a given PC contributes to harmonic problems and implications of installing many such PC's on the power system.

Preliminary Tests

Since there are no established US standards for harmonic distortion currents, we decided to scale the IEC-555-2 standard for use in a 120 V_{ac} system. Ideally, all harmonic current values from the IEC-555-2 standard would increase by a factor of ($230V_{ac}/120V_{ac} = 1.92$). In order to find the actual harmonic data, we tested a Model "C" power supply at 100% load at European ($230V_{ac}/50Hz$), U.S. ($120V_{ac}/60Hz$), and Japanese ($100V_{ac}/50Hz$) standard voltages. The resulting data along with the scaled IEC-555-2 limits are shown in Table 3-2 below:

Table 3-2
Comparison of Typical Power Supply Harmonic Distortion Data to IEC-555-2

Harmonic	Model C @ European Standard $230V_{ac}/50Hz$ (mA/W)	European Harmonic Standard IEC-555-2 (mA/W)	Model C @ U.S. Standard $120V_{ac}/60Hz$ (mA/W)	IEC-555-2 Scaled by $230/120$ for U.S. (mA/W)	Model C @ Japanese Standard $100V_{ac}/50$ (mA/W)	IEC-555-2 Scaled by $230/100$ for Japan (mA/W)
3rd	4.11	3.40	7.50	6.52	8.78	7.82
5th	3.65	1.90	5.92	3.64	6.17	4.37
7th	3.03	1.00	4.10	1.92	3.66	2.30
9th	2.35	0.50	2.50	0.96	2.28	1.15
11th	1.74	0.35	1.62	0.67	2.02	0.81
13th	1.29	0.30	1.44	0.58	1.79	0.69
21st	1.04	0.18	0.65	0.35	0.96	0.41
35th	0.13	0.11	0.14	0.21	0.37	0.25

As can be seen from the test data, the power supply doesn't meet the IEC-555-2 standard at 230 V_{ac} as well as the scaled data at 120 V_{ac} and 100 V_{ac} . We were curious to find out the actual scaling of the harmonic distortion readings at the 230 V_{ac} and 120 V_{ac} operating points and to see if there is any regularity between two different power supplies made by two different manufacturers. The results of this test is shown in Table 3-3.

Table 3-3
Comparison of Actual Harmonic Distortion Scaling Data Between Power Supplies

Model C Tests	3rd Harmonic (mA/W)	5th Harmonic (mA/W)	7th Harmonic (mA/W)
120 V _{ac} , 60HZ	7.50	5.92	4.10
230 V _{ac} , 50 HZ	4.11	3.65	3.03
Actual Scaling Ratio	1.82	1.62	1.35
Model D Tests			
120V _{ac} , 60HZ	7.57	5.83	3.85
230V _{ac} , 50HZ	4.18	3.57	2.81
Actual Scaling Ratio	1.81	1.63	1.37

As one can see from Table 3-3, the actual ratio of harmonic current distortion was remarkably similar between the two units. The actual data generated doesn't imply a simple ratio of the IEC-555-2 limits for the two models of power supplies tested. However, since no other comparison criteria is available, we shall use the scaled IEC-555-2 limits as a comparison against the actual data for the power supplies tested. Clearly, more work needs to be done to either establish a standard for the U.S. or adopt the European standard.

Discussion of Results. All power supplies, except unit GG, were supplied with 100% of nominal input voltage and connected to a resistive load rated at 100% of each unit's capacity. Unit GG was only loaded to 75% due the load bank limitations. Test result data was taken in percent distortion of the fundamental current. In order to normalize all data and compare to the IEC-555-2 standards, the test results were converted to milliAmps/Watt. Figure 3-8 below displays the harmonic current distortion in milliAmps/Watt for the power supplies tested. The IEC-555-2 limits, scaled for 120 V_{ac} operation are included for comparison.

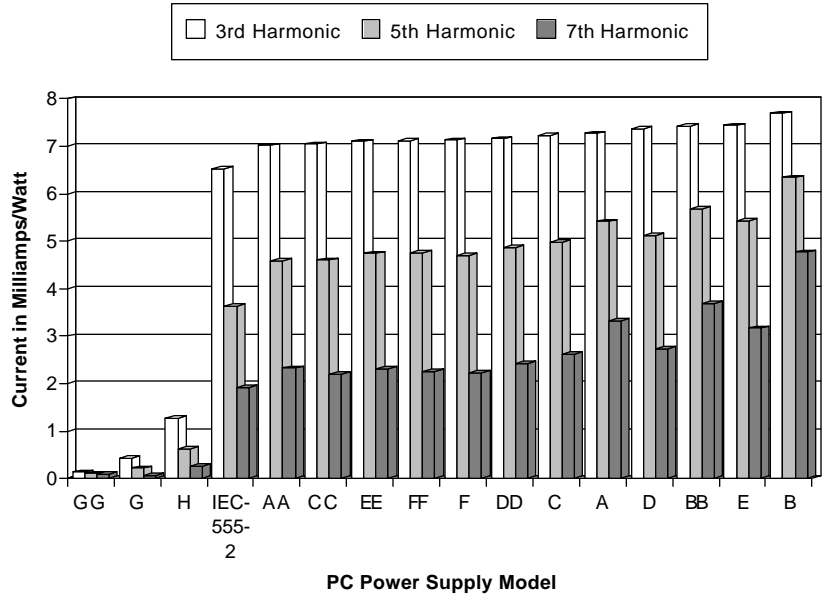


Figure 3-8
PC Power Supply Harmonic Current Distortion Per Harmonic

As can be seen from analysis of Figure 3-8, the power factor correcting supplies are the only devices that meet the scaled IEC-555-2 standards.

The overall total harmonic distortion, I_{thd} , was also recorded for the subject units. Figure 3-9 displays the test results.

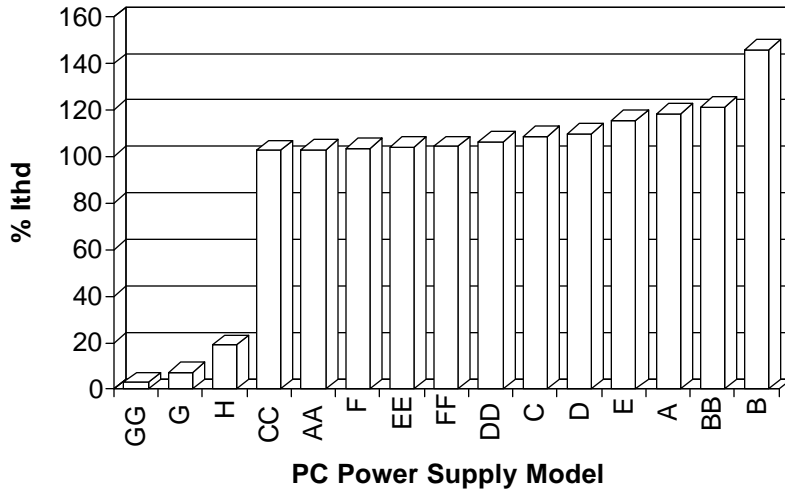


Figure 3-9
 I_{thd} Comparison for PC Power Supplies

Test II. Response to Low Steady-State Input Voltage (*Under-Voltage*)

Overview of Test. Electric power systems are designed and operated so that the steady-state service entrance and utilization voltages normally remain within a design range specified by standards. Under-voltages outside of this range are caused by events such as the switching of heavy loads or capacitor banks. During times of peak load, utilities may lower the transmission line voltages to reduce power consumption. Another more drastic cause of low voltage can occur when one phase in a three-phase power system is lost and the system continues to serve equipment with the remaining two phases. Depending on transformer connections and the load configuration, this condition may result in an extended low-voltage condition. The worst case low voltage level from this condition is believed to be around 58% V_{rms} . PC power supplies should be designed to withstand low voltage conditions and either continue to operate or shut down.

Discussion of Results. The PC power supplies were subjected to an incremental lowering of their input voltage until the units ceased to supply an acceptable output voltage. The +5 volt dc line was monitored as the input voltage was incrementally lowered. Once the power supply ceased to operate or the dc output voltage fell to at least 4.75 Vdc, the input voltage was recorded. Typically, the input voltage was lowered below the operating specifications of the power supply. The response to low steady-state input voltage was conducted at 25% and 100% of each power supplies full load capacity. All models did better than the tolerance envelope established by the CBEMA curve.¹ The CBEMA curve, which establishes 87% of the nominal input voltage ($104.4 V_{ac}$) as the steady-state low voltage tolerance expectation, was developed based on Navy equipment tests and computer power supply studies in 1979. This standard should be revised to account for the more robust low steady-state immunity of today's computer equipment.

During the test, two separate Model E power supplies sustained damage. Model E-1 was damaged at $57 V_{ac}$ input at 25% load while Model E-2 failed at $76 V_{ac}$, 100% load. This response was not observed in the other power supplies tested. Most units either shut down or continued to operate indefinitely at 4.75 V_{dc} . After examining the circuit design, it was found that the regulator IC that regulates the supply voltage of the main PWM IC continues regulating the voltage to maintain PWM operation, resulting input diode bridge failure by over-current. The ride-through capability of this design can be high, but higher current rating diode bridge needs to be used to avoid low-voltage failure. Based on the results of these tests and observations, Model E's manufacturer has redesigned this power supply and is shipping the improved units with their new PCs.

Figures 3-10 and 3-11 display the minimum operating steady-state voltage for the various power supply models.

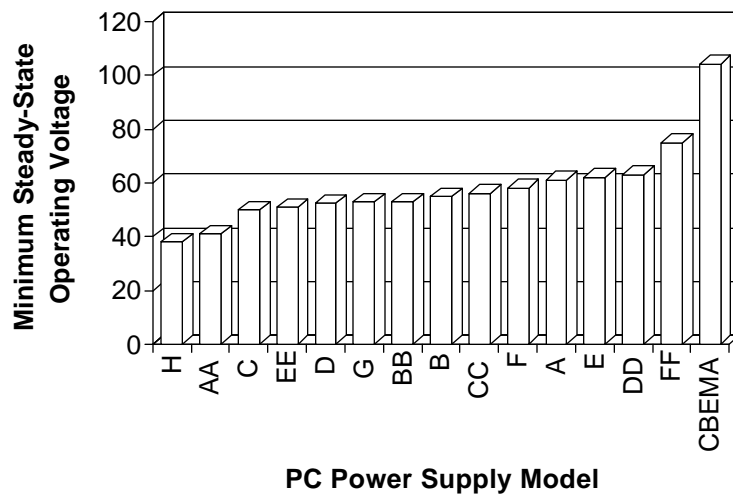


Figure 3-10
Minimum Steady State Operating Voltage at 25 % of Full Load

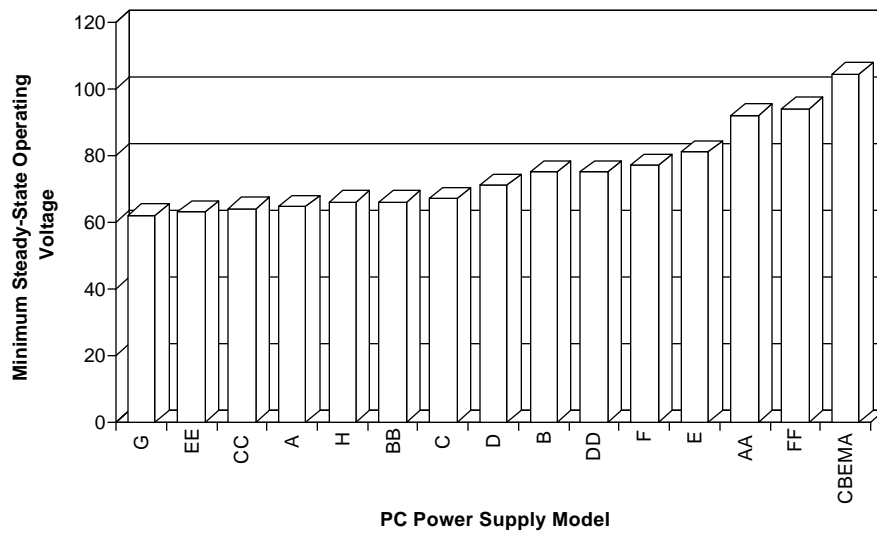


Figure 3-11
Minimum Steady State Operating Voltage at 100 % of Full Load

Test I3. Susceptibility to Voltage Sags and Momentary Outages

Overview of Test. Sags in the line voltage lasting several cycles or longer may result during power system faults and when heavy loads are switched on. These disturbances produce unpredictable results for voltage-sensitive equipment and are common, direct causes of electronic-system upsets or failure.

Discussion of Results.

The results from Test I3 are divided into Older Technology, Current Technology, and Special Technology units and shown graphically in this section. All units tested performed better than the CBEMA curve expectations concerning their steady state low voltage performance. However, for sags with durations from 1-10 cycles, the performance of the UUTs varied. The lower portion of the CBEMA voltage tolerance envelope is shown for the first 30 cycles in Figure 3-12. After 120 cycles, this curve reaches a steady state value of 87%. All models performed better than the CBEMA curve limits at steady state. However, the reaction of each power supply to a short duration sag varied with respect to the CBEMA limits. The results of the testing for the Older, Current, and Special model power supplies is shown in Figures 3-13, 3-14, and 3-15.

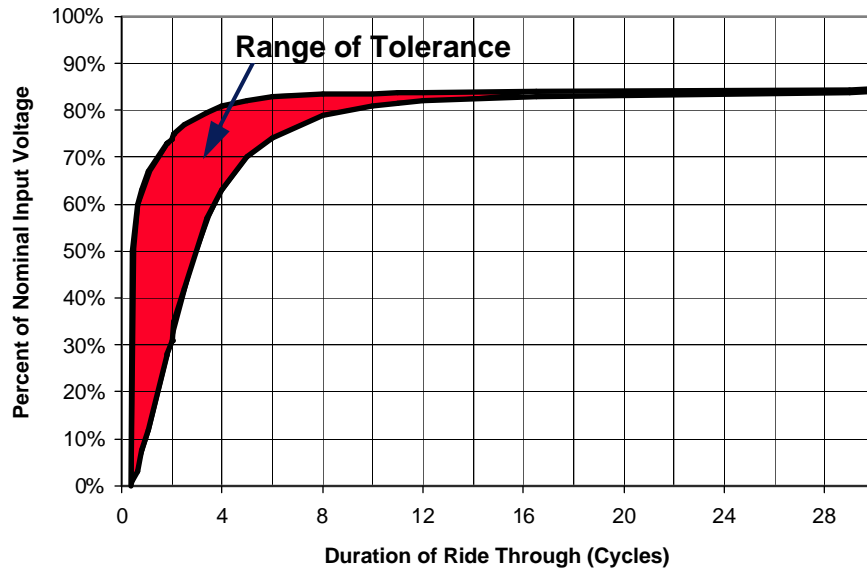


Figure 3-12
CBEMA Curve Low Voltage Tolerance Envelope

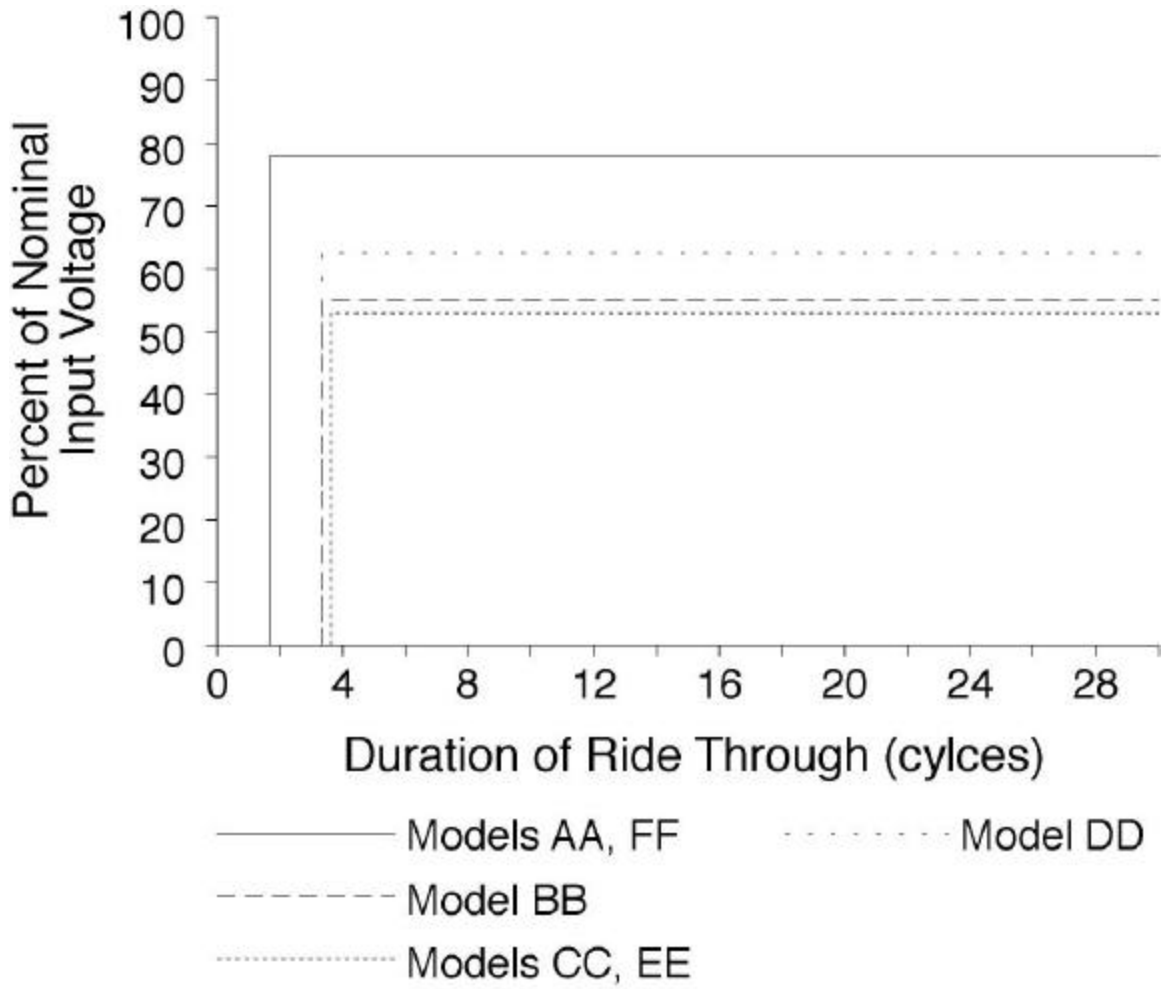


Figure 3-13
Older Model Power Supplies Low Voltage Tolerance Envelope

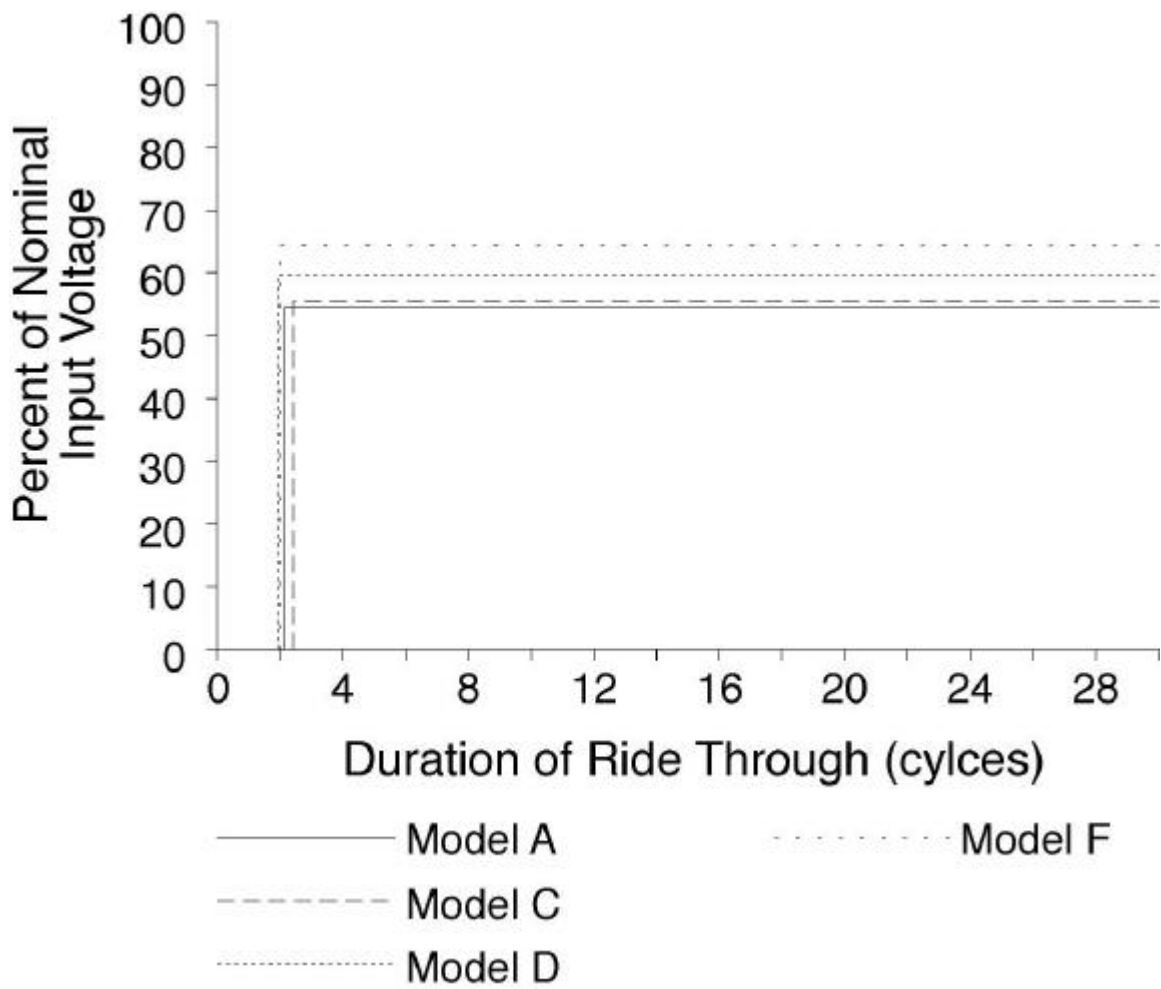


Figure 3-14
 Current Technology Power Supplies Low Voltage Tolerance Envelope

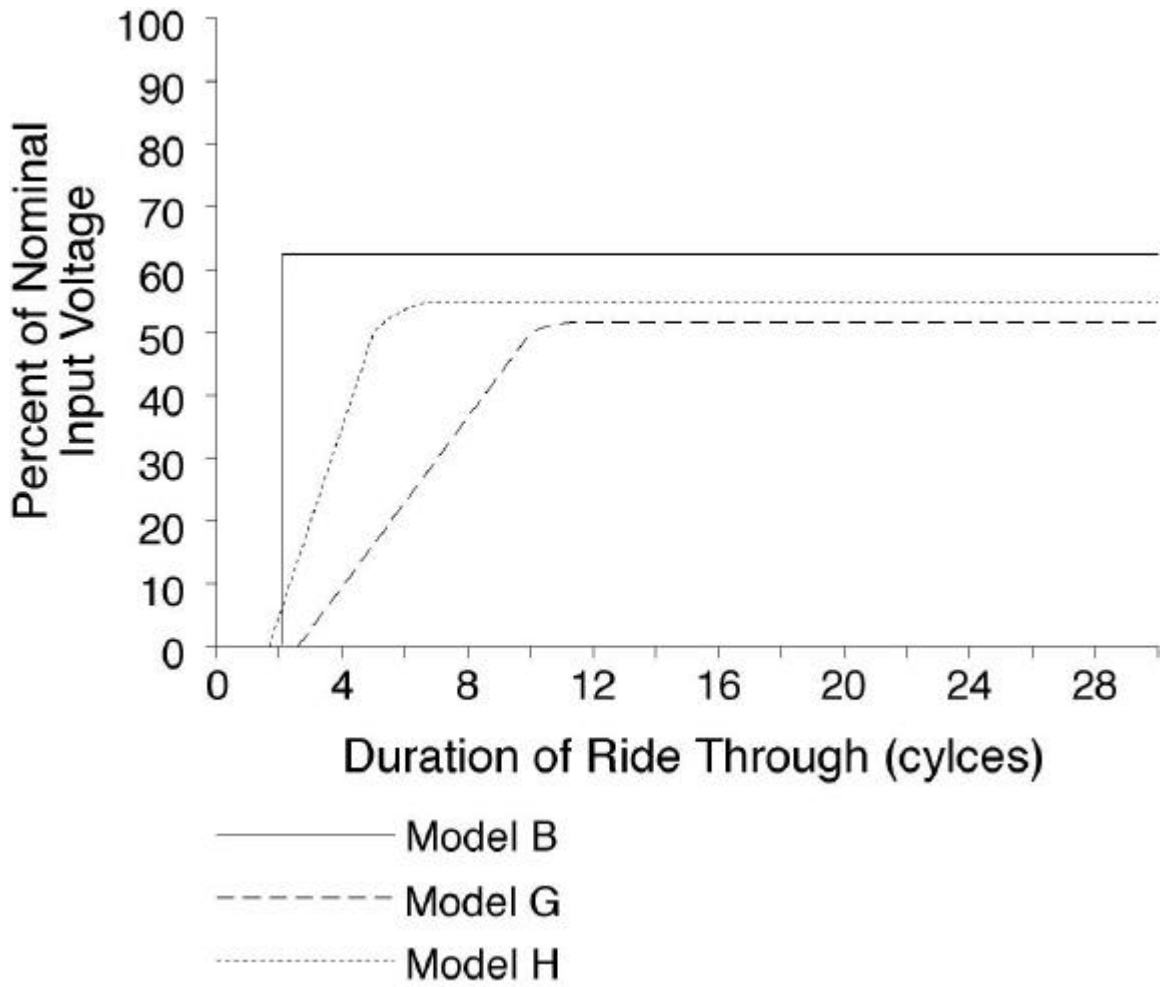


Figure 3-15
Advanced "Special" Technology Power Supplies Low Voltage Tolerance Envelope

Test I4. Susceptibility to Voltage Swells

Overview of Test. Line voltage may increase up to 1.73 times nominal voltage for several cycles during power-system faults on secondary circuits in ungrounded systems or in cases where the neutral becomes ungrounded at the service. Also, the crossing of power lines can produce a temporary over-voltage for a short period.

Discussion of Results. The voltage swell test was conducted at 25% and 100% loads for a 15 Hz duration (250 milliseconds) at 150 Volts RMS. The test results are shown in Table 3-4.

Table 3-4
Voltage Swell Test Data

Model	Load	DC Link Vp	12 V _{dc}	5 V _{dc}
A	25%	202	none	ripple
A	100%	188	none	none
B	25%	382	none	none
B	100%	-----	-----	-----
C	25%	198	ripple	none
C	100%	186	ripple	none
D	25%	200	none	none
D	100%	190	none	none
E	25%	206	ripple	ripple
E	100%	192	none	none
F	25%	372	none	none
F	100%	348	none	none
G	25%	note 1	none	none
G	100%	note 1	none	none
H	25%	note 1	ripple	none
H	100%	note 1	none	ripple
AA	25%	202	none	none
AA	100%	188	none	none
BB	25%	208	none	ripple
BB	100%	196	none	none
CC	25%	196	none	none
CC	100%	180	none	ripple
DD	25%	196	none	none
DD	100%	188	none	none
EE	25%	194	none	none
EE	100%	180	none	ripple
FF	25%	196	none	none
FF	100%	180	none	ripple

Notes:

1. UUT design did not allow access to the link voltage.

Test I5. 500 Hz Ring-Wave Surge Test

Overview of Test. The switching of capacitor banks can cause 5-kHz Ring Wave (defined in ANSI/IEEE C62.41-1991) to appear on high voltage systems. This ring wave can also effect low voltage distribution systems. The impedance of the power system diminishes the standard 5kHz Ring Wave to a 500Hz Ring Wave with a peak magnitude of approximately 150% of V_{nominal} . This wave form may deposit enough energy on the low voltage system to cause failures on single-phase equipment with inadequate surge protection.

Discussion of Results. One model of each power supply was subjected to a 500Hz ring wave across the Line and Neutral terminals. The wave form input and output signals were captured and recorded for each surge event as shown by the typical example in Figure 3-16.

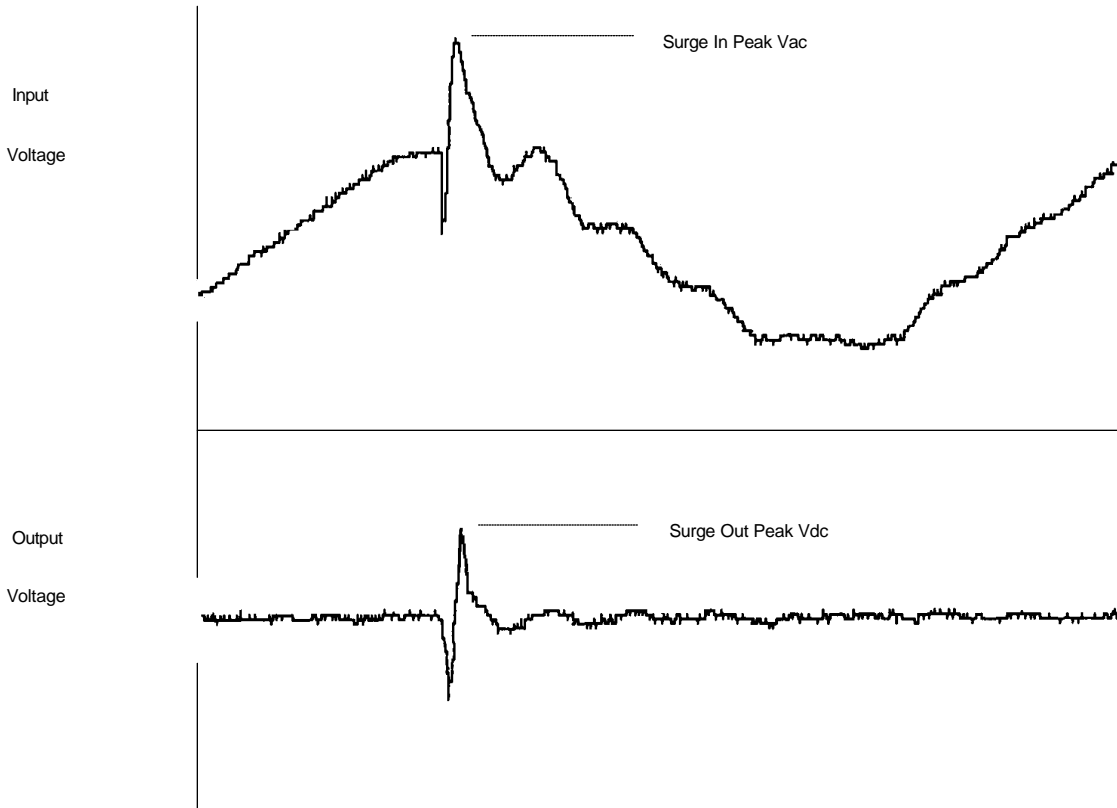


Figure 3-16
Typical 500 Hz Ring-Wave Surge Test

There were no power supplies damaged during this test. In addition, all units continued to operate normally within 1/2 cycle of the disturbance event. Table 3-5 below summarizes the results of this test.

Table 3-5
500 Hz Ring Wave Data

Model	Surge In (Peak V_{ac})	Surge Out (Peak V_{dc})	% disturbance	Continuous Operation?
A	392	6.4	28%	Yes
B	336	6.24	25%	Yes
C	304	6.32	26%	Yes
D	-----	-----	note 1	
E	496	6.24	25%	Yes
F	380	6.32	26%	Yes
G	-----	-----	note 1	
H	-----	-----	note 1	
AA	368	6	20%	Yes
BB	360	6.24	25%	Yes
CC	368	5.84	17%	Yes
DD	360	5.84	17%	Yes
EE	368	5.84	17%	Yes
FF	360	6.4	28%	Yes
GG	368	6.48	30%, note 2	Yes

Notes:

1. Unit not tested.
2. Unit tested at 75% load.

Test I7. 0.5 μ s-100 kHz Ring Wave Surge Test

Overview of Test. Ring Waves are the most frequently observed transient over-voltages occurring in low-voltage power systems. Even a unidirectional impulsive surge on overhead lines will induce oscillatory transients at the residential service entrance. The ANSI/IEEE C62.41 Standard 100kHz Ring Wave has a rise time of 0.5 μ s. A short rise time means fast dv/dt , which can fail or sporadically turn on semiconductors.

Discussion of Results. In this test, the power supplies were subjected to a ring wave across the Line-Neutral, Line-Ground, and Neutral to Ground in three separate tests. All devices tested continued to operate after the disturbance. This test will be much more conclusive in the future testing when the effect on a PC system will be explored (lock-ups, etc.). An example Line-Ground surge wave from this test is shown in Figure 3-17.

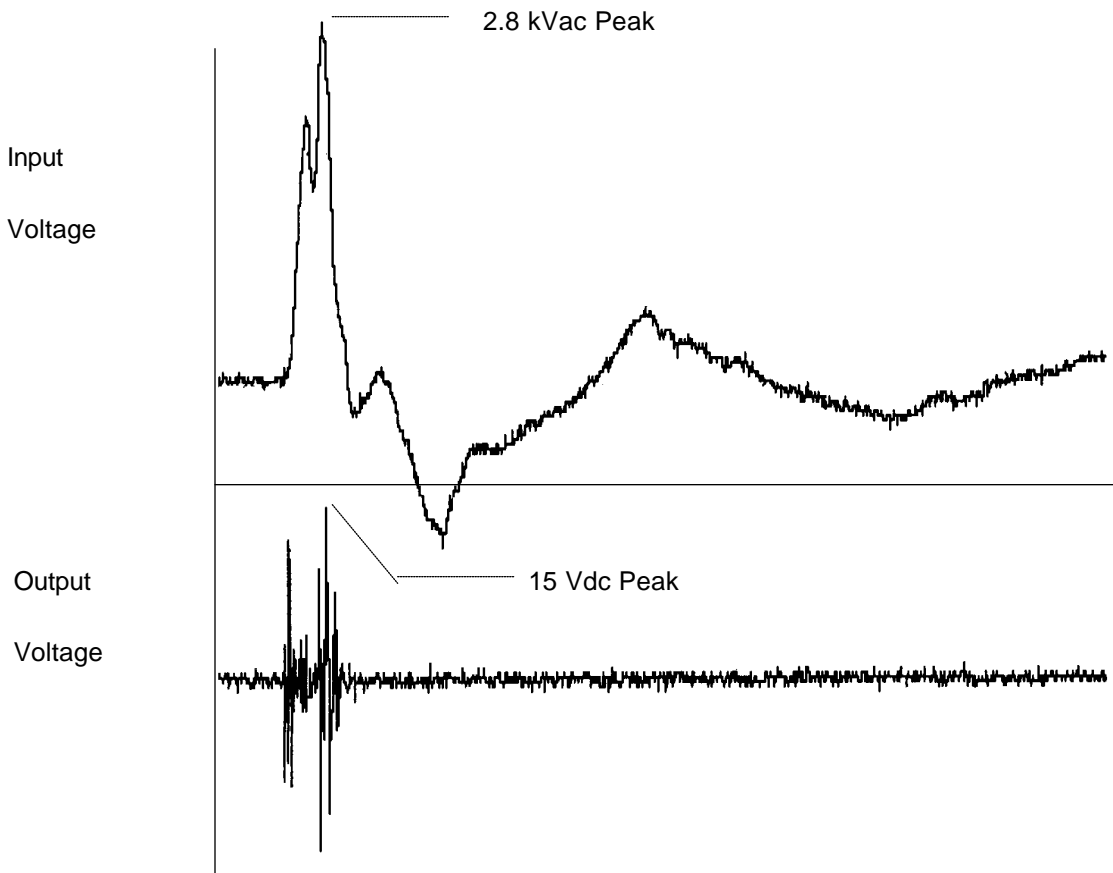


Figure 3-17
Typical PC Power Supply Response to a 0.5 μ s-100 kHz Ring Wave

Test I9. 1.2/50 μ s-8/20 μ s Combination-Wave Surge Test

Overview of Test. High energy unidirectional transients caused by switching of capacitor banks, faults in the power network and lightning strokes are known to exist in low-voltage systems and can cause failure of PC's.

Discussion of Results. Combo waves were injected into the PC power supplies across both the Line-Neutral and the Line-Ground terminals in two separate tests. In all cases the PC supplies tested survived the tests and continued operating. A typical combo wave for a Line-Neutral signal is shown in Figure 3-18.

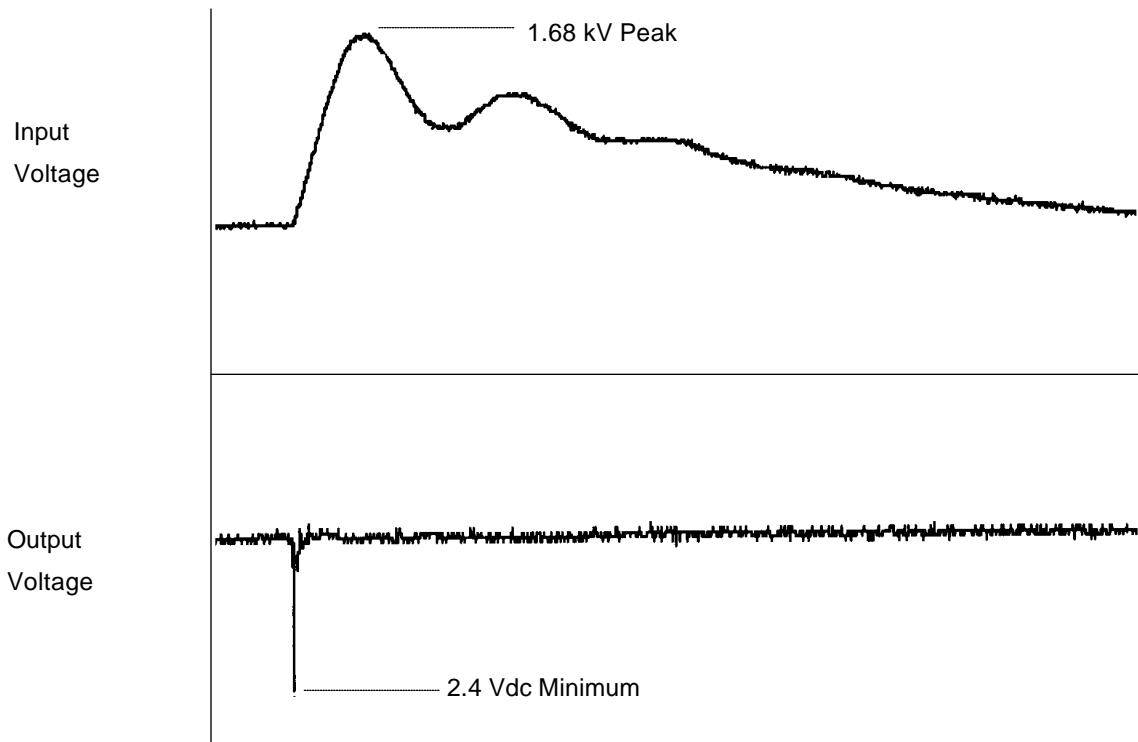


Figure 3-18
Typical Line-Neutral Combo Wave PC Power Supply Response

As can be seen from the typical results, the power supplies tested continued to operate normally after the disturbance. It is unclear how the 2.4 Vdc dip in the output voltage (duration in nano second range) would actually effect a PC system.

Test I10. Electrical Fast Transient (EFT) Burst-Wave Surge Test

Overview of Test. The EFT Burst Wave, typically generated from switching of small inductive loads, relay contacts bouncing (conducted interferences) and switching of HV-switchgear (radiated interferences). The significant characteristics of these transients are fast rise time, short duration, low energy but with high repetition rate. The voltage level in residential environment might be lower than that in an industrial environment. For the purposes of the test, a 4kV voltage burst levels were injected into the PC power supplies.

Discussion of Results.

All units continued to operate during and after the EFT test. The results of this test are not conclusive. The results of such a test will be more informative when conducted on an actual PC system.

Test I4' Swell to Fail Tests

Overview of Test. The High Steady-State Input Voltage and Voltage Swell Response tests were combined into one test. The purpose of this test is to determine the over voltage tolerance limits to define the upper portion of the voltage tolerance envelope for the UUTs. The technician conducted the test by "sneaking up" on the failure point. Both the peak swell voltage (Vp) and the swell duration (cycles) were adjusted to find the data points.

Discussion of Results. Because of the potential for damaging the power supply units, this test was conducted last. Only the current technology units were tested. The test results show that the models tested were well beyond the expected levels indicated by the current CBEMA curve. The test results from the units tested are summarized in Table 3-6.

Table 3-6
Swell to Fail Test Data

MODEL	Vp	Duration (cycles)	RECOVERY?	RESULT
A-1	400	3	NO	NO DAMAGE
A-2	300	15	NO	DAMAGED SPD & FUSE
B-4	390	499.5	N/A	NO EFFECT
B-4	450	12.5	YES	NO DAMAGE
B-4	500	2.5	NO	NO DAMAGE
B-4	520	499.5	N/A	NO EFFECT
B-4	590	13	NO	NO DAMAGE
C-3	380	2	N/A	NO EFFECT
C-3	390	5	NO	NO DAMAGE
D-2	390	4	N/A	NO EFFECT
D-2	410	2.5	NO	INVERTER SWITCH DAMAGED
E-1R	260	450	N/A	NO EFFECT
E-1R	290	4	N/A	NO EFFECT
E-1R	310	2	YES	NO DAMAGE
E-1R	360	1.5	YES	NO DAMAGE
E-1R	300	3	YES	NO DAMAGE
E-1R	300	5	YES	NO DAMAGE
E-1R	300	38	NO	DAMAGED SPD & FUSE

notes:

1. SPD - Surge Protection Device
2. N/A result in the "Recovery" column indicates that the UUT was not upset.

3.4

Identification of Circuit Topologies and Their Critical Components --

This task identifies the critical components that effect the performance areas of interest and will document the range of different types in use. The specific design or technology differences, and the factors that are important to performance will be identified for each concern. The following table lists the application concerns, critical components and the performance range of different types found to be used in the power supply investigated.

Table 3-7 lists all the circuit topologies and their critical components that affect the power supply performance. For efficiency consideration, the 5V output diode consumes the most percentage of the power because its voltage drop relative to its output level is high. This 5V output diode loss can be reduced by 1 to 2 percent with a latest available Schocctky component, but its associated cost will be increased significantly if the quantity is not sufficiently high.

Table 3-7
Identification of Critical Components

Critical components and typical range of technology in use that impact power supply application concerns		
<i>Application Concerns</i>	<i>Critical Components</i>	<i>Types or Range of Values</i>
1. Efficiency		
percent losses	Circuit topologies	Buck converter with reset winding; Buck converter with RCD clamp; Flyback converter; Half bridge converter; Push-pull converter.
4~8%	Switching devices	Bipolar transistors; Power MOSFET
5~9%	Output 5 V diodes	Schocttky (typically 45 V, 30 A)
1~2%	Output 12 V diodes	Schocttky, ultra fast recovery
1~2%	Output inductors	none
1~3%	Input diode bridge	600 V, 3 A ~ 5 A
1~2%	Input EMI filter inductors	tbd
2~4%	Transformers	E-core, Toroid
1~2%	Fan	1.44 W ~ 3.6 W with or w/o temp. control
0.5~3%	Thermistor	2 Ω ~ 9 Ω at room temp.
2~5%	Snubbers	RCD for all switching elements
2~6%	Control circuits and others	varies
2. Impact on Power Source		
Harmonics	DC link capacitor	330 μ F ~ 1000 μ F
	Boost converter	with or without
Filtering	EMI filters	20dB/dec @ $f_c = 9$ kHz ~ 260 kHz
		low pass or band pass filter
3. Immunity to Power Source		
Input voltage range	DC link capacitor	2 @ 330 μ F ~ 1000 μ F, 200 V
	Boost converter auto range	with or without converter
Sag Ride through	DC link capacitor	2 @ 330 μ F ~ 1000 μ F, 200 V
	PWM chip supply	By a separated 60 Hz rectifier By a separated switching regulator By output 12 V feedback
Swell upset and failure	Surge suppresser (dc x 2)	2 @ > 250 Volts rated
	Y caps	2 @ 600 V, 1000 pF ~ 20 nF
	X caps	2 @ 250 Vac, .1 ~ 1 μ F
Surge upset and failure	Feedback isolation circuit	Transformer or Optocoupler
	ac surge suppresser	none is there
	Grounding at 5Vdc	reference to ac chassis ground varies
	Grounding at 12 Vdc	reference to ac chassis ground varies

Also see the characterization of critical components section on the lab data sheet #0.

3.5

Access technology performances and make recommendations

This task provides a technology assessment and show what can be expected in performance from these technologies relative to each of the power supply application concerns. Best performing circuits and components will be identified, as well as the expected effect on cost and efficiency. Only existing available technology will be considered in specifying enhanced power supplies. The following table lists the application concerns, the recommended technology that address these concerns and the expected cost and efficiency impacts.

Table 3-8
Recommended Technology for PC Power Supply Performance Improvement

Recommended technology to address power supply application concerns and expected effect on cost and efficiency				
<i>Application Concerns</i>	<i>“Baseline”</i>	<i>Alternate Technology</i>	DCost	D h
1. Efficiency				
	70%	80%		
	Buck converter	Buck converter / active clamp;	tbd	tbd
	800 V MOSFET	600 V MOSFET + active switch circuit	\$0 \$3	5% -1%
	45V, 30A diode	45 V, 60 A Schottky diode	\$.50	2%
	200V, 10A diode	90 V, 10 A Schottky diode	\$0	.5%
	Thermistor	2 Ω at room temp.	\$0	1%
	Fan w/o control	1.44 W with temp. control	\$1	1%
2. Impact on Power Source				
Harmonics	90%	10%		
active filter	simple rectifier	add a front-end boost converter	\$6	-2%
passive filter	at front-end	add series inductance at tbd	tbd	tbd
series inductance	very small (EMI)	3% @ 60 Hz, maybe 50% thd	\$6	-1%
Filtering	kHz Notch	move to .100 kHz or flat resp.		
	EMI filter	different EMI filter?	tbd	tbd
3. Immunity to Power Source				
Input voltage range	120 or 240 ± 20%	auto ranging 60 to 240Vac		
	unregulated dc-link	boost converter	\$6	-2%
Sag Ride through	1-2 cycles	10 cycles (166ms) @ Vrms = 0		
ripple capacitor & switching regulator &	330µF DC cap.	2 @ 470 µF DC link cap.	\$1	--
h-f transformer ratio & control power source	50% duty cycle	90% duty cycle/active clamp	tbd	
	approx. 20/1	reduce ratio to 10/1	tbd	
	Vpwm-chip sags	add regulator for control power	\$3	
Swell upset and failure	survive @ 150%	survive @ 150%		
surge suppresser dc-link	>200 V	no change for now	--	
x and y capacitors	250 Vac, 600Vdc	no change	--	
Surge upset and failure	problems @ 1kV	immune up to 3kV/1.5kA		
surge suppress front end	none	needs 2-150-V MOV	\$.60	--
series inductance	very small (EMI)	1% @ 60 Hz	\$4	-1%
cap. or zener at 5Vdc	varies	add tbd	tbd	

In a future task new innovations and potential advances in technology will be looked at to further improve power supply performances. The market conditions, cost and expected trends that are likely to impact the design or technology selection will also be investigated.

APPLICATIONS OF RESULTS

4.1

Cost of Harmonics

In order to evaluate the impact of the harmonic and reactive current flow in a typical commercial building, a building wiring model was developed. Figure 4-1 illustrates the single-line diagram of this commercial building ac distribution system which was adapted for the IEEE Std 1100, *The Emerald Book*. The system contains both linear and nonlinear loads. Harmonic distortion is severe at the terminals of the nonlinear loads, but it tends to be smoothed out by three-phase connections and other linear loads. This figure, published in the *IEEE Emerald Book* shows current waveforms at different line sections.

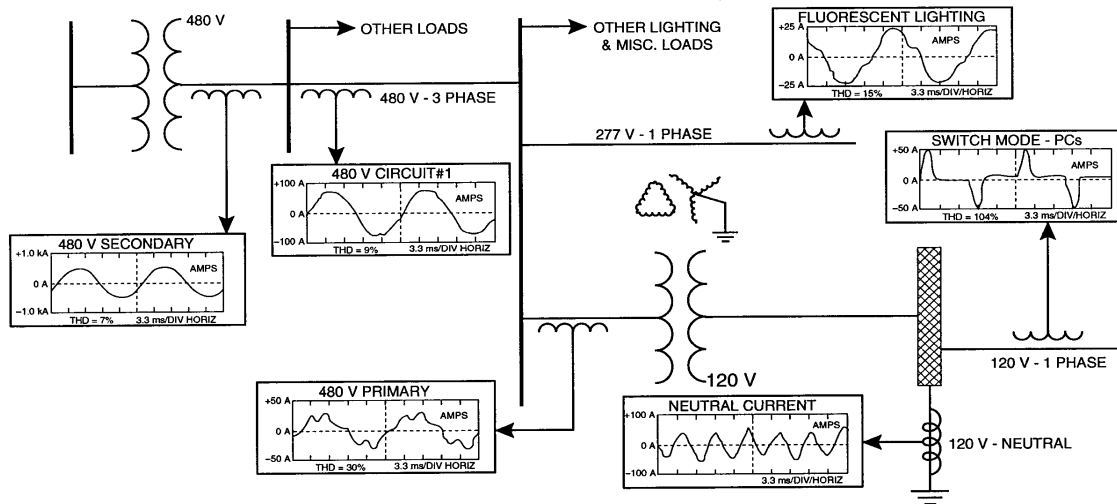


Figure 4.1

Example harmonic currents in a typical commercial building.

The cost-benefit analysis compares the estimated cost of harmonic- and reactive-current compensating equipment to the calculated cost of building power system losses when these currents are not compensated and are allowed to flow. Building power system losses are based on the previous determination of harmonic-related losses for the 1000 kVA commercial building model. This analysis assumes 60 kW of office electronic load. The cost of energy is set at \$.10/kWH. It is assumed that the distributed personal computers, 240 computers on 120 branch circuits, and other related electronic office equipment, operate 12 hours per day 365 days per year.

Each compensating equipment option is situated in the building power system to achieve its maximum effectiveness relative to reducing harmonic-related losses. Table 4.1 summarizes the energy saving of different harmonic compensation methods. It inventories the potential loss reductions in the different line segments and in the step-down transformer of the building power system. These energy loss reductions will vary depending on load harmonic content as well as the pe and the location of the compensating equipment.

This table lists the energy saving for the case of 100 percent current THD at the load and 60 kW of switch-mode power supply load. The saving is based on the reduction in wiring losses as a percent of the switch-mode power supply loading. Without any compensation the losses for a 60-kW switch-mode power supply load would be 8150 watts or 12%. For comparison, powering a linear load may result in losses of about 4-5% in the building wiring.

Table 4.1
Energy saving by different harmonic compensation methods

Location Options	At Service Entrance	At Sub-Panels or Load Center Level			At Branch Circuit or Cord Connect		Built into Load Equipment	
		Active Filter	Passive Filter PCRFB	Neutral I-Trap Xformer	Passive Filter SCRF	Passive Filter PCRFB	Built-in Boost Converter	Built-in Inductor
Compensation Method/ Configuration	Passive Capacitor Bank 1×200 kVA	Active Filter 1×60 kVA	Passive Filter PCRFB 1×60 kVA	Neutral I-Trap Xformer 1×60 kVA	Passive Filter SCRF 120×0.5 kVA	Passive Filter PCRFB 120×0.5 kVA	Built-in Boost Converter 240×0.25 kVA	Built-in Inductor 240×0.25 kVA
Saving at I_1 (W)	0	0	0	0	1241	1241	1320	579
Saving at I_2 (W)	0	712	664	619	664	664	712	310
Saving at I_3 (W)	0	53	48	42	48	48	53	30
Saving at T_1 (W)	0	2747	2360	1006	2360	2360	2747	1004
Total Saving for 60 kVA load (W)	0	3512	3072	1667	4312	4312	4832	1923
% Saving / 60 kVA	0	5.85%	5.12%	2.78%	7.19%	7.19%	8.05%	3.21%

Table 4-2 summarizes the total losses and savings with and without reactive compensation. The results indicate that the most effective energy saving compensation method is the built-in boost-converter circuit in each computer power supply. This method reduces losses from 13.6% to 5.6% and provides an energy savings of about 8% in the studied case--100 percent current THD, 53 percent loading of the system capacity, and 50 percent operating hours.

This is not an extreme case; rather, it is believed to be somewhat typical in that all system components are reasonably loaded if the load is more linear. The losses for the case of a linear load in the same building wiring scenario are expected to be about 5%. In other

cases where the current *THD* is higher than 100, or when the loading is closer to the system's full capacity, the energy savings from reactive current compensation will be more substantial.

Table 4-2

Power system loss reduction for different compensation methods and locations for 60 kVA loading.

Compensation Location Options	Base Case	At Sub-Panels or Load Center Level			At Branch Circuit or Cord Connect		Built into Load Equipment	
		Active Filter	Passive Filter PCRFB	Neutral I-Trap Xformer	Passive Filter SCRF	Passive Filter PCRFB	Built-in Boost Converter	Built-in Inductor
Compensation Method/ Configuration	Losses if No Reduction Method is Used	1x60 kVA	1x60 kVA	1x60 kVA	120x0.5 kVA	120x0.5 kVA	240x0.25 kVA	240x0.25 kVA
Saving at I_1 (W)	2647	0	0	0	1241	1241	1320	579
Saving at I_2 (W)	921	712	664	619	664	664	712	310
Saving at I_3 (W)	289	53	48	42	48	48	53	30
Saving at T_1 (W)	4322	2747	2360	1006	2360	2360	2747	1004
Total saving for 60 kVA load (W)	0	3512	3072	1667	4312	4312	4832	1923
Total losses with compensation (W)	8178	4666	5106	6511	3866	3866	3346	6255
Losses / 60 kVA	13.63%	7.78%	8.51%	10.85	6.44%	6.44%	5.58%	10.4%
Saving / 60 kVA	0%	5.85%	5.12%	2.78%	7.19%	7.19%	8.05%	3.21%

4.2

IEEE-CBEMA Immunity Curves

For most personal computer's, line voltage is the factor which has the most effect on power quality. The tolerance of PC's to power line voltage fluctuations should roughly follow a voltage envelope as shown in Figure 4-2. There are variations in these limits for equipment made by different manufacturers; however, the basic shape is applicable to all. This envelope has been accepted by the Computer Business Equipment Manufacturer's Association (CBEMA) and was adopted by IEEE Standard 446 "Recommendation Practice for Emergency and Standby Power Systems for Industrial and Commercial Application".

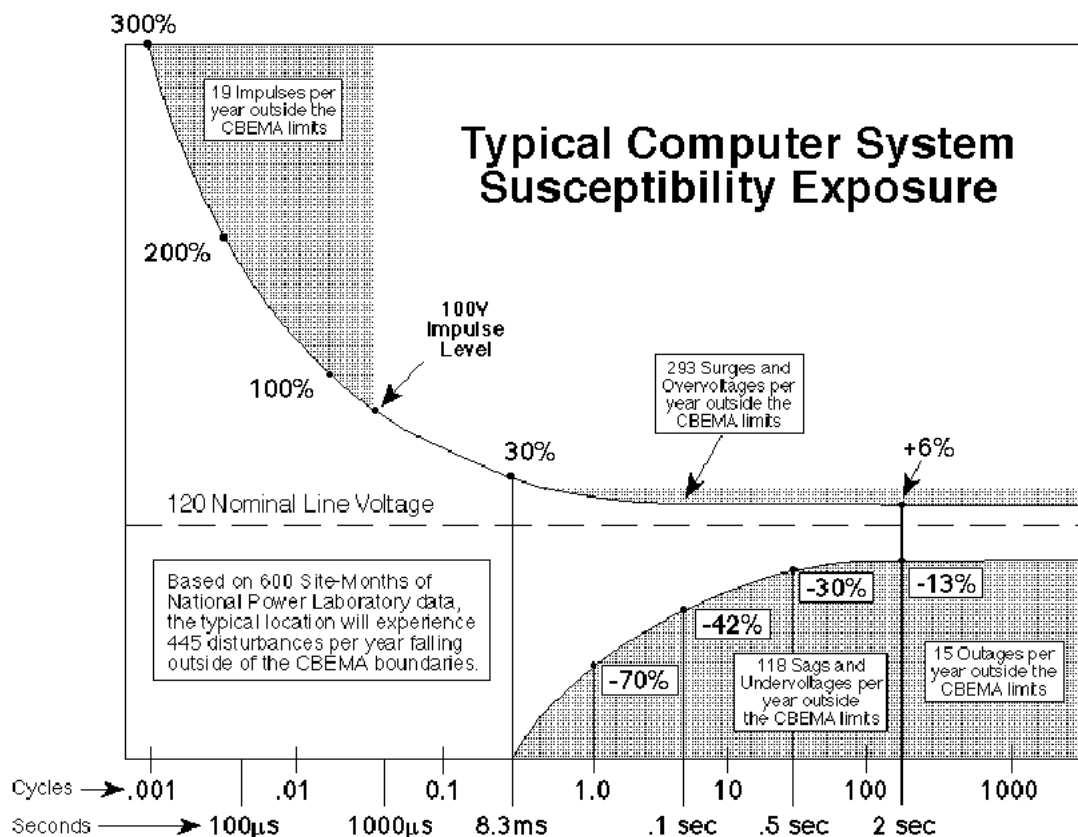


Figure 4-2
Typical Computer System Voltage Tolerance Envelope

Figure 4.3 compares the low voltage test results of three selected models and the CBEMA curves. The three models, DD, A, and G represent “old design,” “new design,” and “special design,” respectively. All three models meet the CBEMA steady-state limit.

The short duration (under 6-cycles or 0.1-second interruption) sag performance of the two conventional designs (old and new) fall into the tolerance range of the CBEMA curves. The specially designed model (meaning with a front-end boost converter) perform exceedingly better than the lower part of the CBEMA curves.

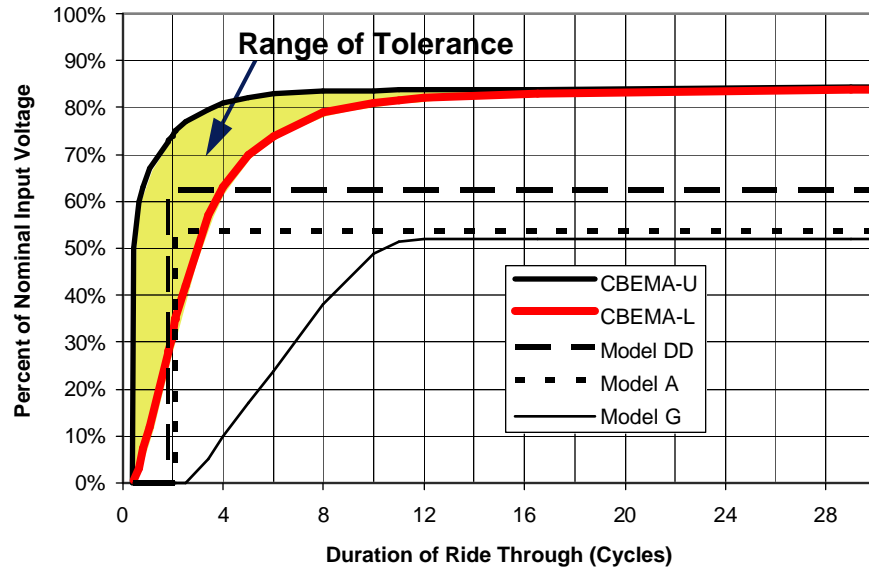


Figure 4-3
Voltage-Tolerance Test Results Compared to Low-voltage CBEMA Curves

FUTURE WORK

Power supply ac interface issues involve interference and immunity between the utility ac power system and the high frequency dc-to-dc power converter. Major issues include (1) harmonics and EMI interferences which are produced by the power supply and interfere with the ac system and (2) voltage variations and interruptions which are caused by the ac system and interfere with the power supply. Test results found that the specially designed power supplies with a front-end boost converter outperformed the conventional rectifier-capacitor interface in both interference and immunity issues. The only concern is the energy performance with the added boost converter. Although a past study indicated that the system energy cost can be reduced with an improved power factor, the individual power supply test does not reflect such system cost reduction. Further tests are required to justify the system energy performance with different power supply designs.

The trend that the computer industry is moving from 5-V logic to 3.3-V or lower voltage logic creates another concern about the energy performance of the power supplies. Because the forward voltage drop of silicon diodes cannot be reduced, the drop of the voltage level means a relatively higher loss in the power supply output rectifiers is unavoidable. Using synchronous rectifiers for the power supply output may improve the energy performance for lower voltage systems, the incurred cost penalty could prevent the OEM from making it. The use of lower voltage logic also implies a tighter EMI tolerance. There may be a potential benefit from using lower voltage logic, that is, the use of high energy density ultra capacitors for ride through improvement. Like the conventional batteries, the voltage of the ultra capacitor cell is typically around 2V. High capacity capacitors can be easier obtained at lower voltage levels, and the low voltage power back up can be easier implemented.

Intelligent energy management system based on the CPU computing needs could be a new trend in the computer power supply design. Such systems have been found in most portable computers. The efficiency of the power conversion itself may remain the same, but the computer system efficiency may be improved over a long period of time with energy management. Such system efficiency improvement also requires further tests to justify.

Part I of the PC Host Utility Project focused primarily on the effect of power quality disturbances on switch mode PC power supplies. The results of these tests has led to a better understanding of the immunity of the PC power supply. In the course of testing, the power quality disturbances that damage, upset, and have no effect on a PC power supply have been identified. Armed with this knowledge, the next logical step is to investigate the effect of disturbances on:

1. PC systems
2. PCs and their Peripheral Device Interface Ports

In the testing of a PC system, many of the same tests would be conducted. However, the emphasis of these tests would be to see if the PC is damaged or any PC software tasks are interrupted during the testing. The primary goal of these tests would be to identify the disturbances that can lead to PC "lock-up". Everyone who has used a computer has experienced a keyboard "lock-up" at some time. Once thought to be due primarily to memory management problems within the PC, it is possible that some of these problems may actually be due to power quality disturbances.

The testing of PCs and their Peripheral Devices would explore the effect of a power quality disturbance on Local Area Network (LAN) communications to devices such as printers and other computer systems. These tests will focus on the frequency of LAN communications errors and collisions during a disturbances as compared to normal operation.

Through this study, several areas of advanced power electronics technology development related to ac interface issues have been identified for enhancement of the power supply immunity and alleviation of the interference. Normally power conversion efficiency can be improved by employing soft switching or resonant power conversion techniques such as zero-voltage transitioned boost converters, active-clamped forward converter with soft-switching, and synchronous rectifiers. All these new technologies are surrounded by the most fundamental issue – cost, and the “cost” can only be driven down by a large quantity. The question is which comes first, technology or quantity. In the near future, with possible enforcement of new power quality standards such as IEC555-2 and CBEMA curves, new power supply product development is needed for compliance of these upcoming standards.

REFERENCES

- [1] Thomas S. Key, "Diagnosing Power Quality-Related Computer Problems", IEEE paper IPSD 78-12, August, 1979.
- [2] J. Lai, D. Hurst, and T. Key, "Switch-Mode Power Supply Power Factor Improvement Via Harmonic Elimination Methods," conference record of Applied Power Electronics Conference, Dallas, TX, March 1991.
- [3] IEEE Std 519-1992, IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, revision of IEEE Std 519-1981, IEEE Guide for Harmonic Control and Reactive compensation of Static Power Converters.
- [4] IEC Sub-Committee 77A, Low frequency phenomena, Secretariat 90 (1993), "Disturbances Caused by Equipment Connected to the Public Low-Voltage Supply System. Limits concerning harmonics currents for equipment having an input current up to and including 16A per phase."
- [5] IEEE Emerald Book, *IEEE Recommended Practice for Powering and Grounding Sensitive Electronic Equipment*, IEEE Std 1100-1992.
- [6] R. Zavadil, et al, Analysis of Harmonic Distortion Levels in Commercial Buildings, Proceeding: First International Conference on Power Quality, PQA 1991
- [7] R. Gretsche, "Harmonic Distortion of the Mains Voltage by Switched-Mode Power Supplies—Assessment of the Future Development and Possible Mitigation Measures," EPE Aachen, 1989, pp. 1255 - 1260.
- [8] T. S. Key and J. S. Lai, "Comparison of Standards and Power Supply Design Options for Limiting Harmonic Distribution," *IEEE Trans. on Ind. Appl.*, Vol. IA-29, No. 4, Jul./Aug. 1993, pp. 688–695.
- [9] Mohan Mankikar, "Power's Unpaved Future," *Electronic Engineering Times*, May 22, 1992, p. 72.
- [10] J. S. Lai, et al., "High Energy Density Double-Layer Capacitors for Energy Storage Applications," *IEEE AES Magazine*, April 1992, pp. 14 – 19.

APPENDICES

- A. Units Tested
- B. Circuit Topology Comparison
- C. Test Procedure for Information Technology Equipment to merit Energy Star Label
- D. Energy-Efficient Microcomputers: Guidelines on Acquisition, Management, and Use, U.S. General Services Administration, July 1994, Appendices A-D.

Appendix A

Units Tested

Table A. 1 lists the selected power supply models and their manufacturing associated information. A total of 15 power supply models were tested. Among them, six models were from PEAC inventory, dated 1989 or older. These power supplies are categorized as the “older design” for PC or PC compatible computers. Six PC power supply models were acquired after the project started, dated between 1992 and 1994. These power supplies are categorized as “current manufacturer” or “current mngr” shown in Table A. 1. Three “specialty” power supply models, also dated between 1992 and 1994, are for workstations or for general-purposed uses. These models are all designed with a front-end boost converter to eliminate the harmonics generated from the rectifier-capacitor circuit.

Table A.1
Selection of PC Manufactures and Power Supply Models

Model	PS Category	Date	Made in	Watts	Model/Features	Used in
BB	older design	1985	Mexico	130	Std IBM part	XT
EE	older design	1986	Hong Kong	175	Std IBM part	AT
AA	older design	1986	USA	200	Std Compaq part	286
FF	older design	1988	Taiwan	200		286
DD	older design	1989	Korea	130		286
CC	older design	1987	Malaysia	200		386
A	current mngr	1994	Taiwan	150		486
E	current mngr	1994	Taiwan	145		486
B	current mngr	92/93	Taiwan	150	Energy Star	486
C	current mngr	1993?	Malaysia	200	Super 2200	486
D	current mngr	93/94	Taiwan	150		486
F	current mngr	1994	Taiwan	200		486
G	specialty	1994	Taiwan	150	low harmonic	ws
H	specialty	1992	Japan?	140	low harmonic	ws
GG	specialty	1994	Mexico	600	low harmonic	ws

Table A.2 lists the extent and sequence for testing related to specific power supply types. The test order starts from steady state performance characterization, then transient surge response test, and finally the swell test for the upper CBEMA curve.

Table A.2
Specific Test Schedule

as of 11/9/94

Test Order	Test Description	Testing as of Oct 10			Testing by Nov 31		
		Old	New	Special	Old	New	Special
0	base line	1 each	1 each	1 each	1 each	1 each	1 each
1.1-1.4	steady state	1 each	1 each	1 each	1 each	2 each	2 each
1.5	N-G tests	1 each	1 each	1 each	1 each	1 each	1 each
1.6	distorted Vrms	0	0	0	1 each	1 each	1 each
2.	input impedance	1 each	1 each	1 each	1 each	1 each	1 each
3	low voltage trip	select 6	select 4	select 2	1 each	1 each	1 each
4	sag response	select 6	select 4	select 2	1 each	1 each	1 each
5.1	capacitor switch response	1 each	1 each	1 each	1 each	1 each	1 each
5.2-5.4	ring-wave surge response	select 2	select 2	0	1 each	1 each	1 each
5.5-5.6	noise burst response	0	0	0	1 each	1 each	1 each
5.7	lightning surge response l-n	select 2	select 2	0	1 each	1 each	1 each
5.8	lightning surge response l-g	select 2	select 2	0	1 each	1 each	1 each
5.9	surge response n-g- 1kVmax	select 2	select 2	0	1 each	1 each	0
5.10	lightning surge stress test	0	select 1	0	only 1	1 each	0
6	swell response	select 6	select 4	select 2	1 each	1 each	1 each
7	swell to fail (several points)	0		0	only 1	8 point	0

Appendix B

Circuit Topology Comparison

B.1

Complete Block Diagram of a Computer Power Supply

A computer power supply consists of two main sections: (1) ac-to-dc interface and (2) dc-to-dc converter. The ac-to-dc interface is traditionally designed with an EMI filter and a rectifier-capacitor circuit. The EMI filter is to prevent the switching noise, which is generated from the dc-to-dc converter stage, from conducting back to the mains to interfere with other electronics equipment. The rectifier circuit is to convert the ac input voltage to an unregulated dc voltage with the capacitor filter to smooth the voltage ripple. A selecting switch is normally designed to allow dual ac input voltage operation so that the product can be sold to different countries. When operating at the low input ac voltage (115 Vrms nominal), the rectifier is in half-wave charging mode to obtain a dc bus voltage at about 300 V. When operating at the high input ac voltage (230Vrms nominal), the rectifier is in full-wave charging mode to obtain the same level of dc bus voltage. This unregulated dc bus voltage is then converted, through a dc-to-dc converter, to low voltages ($\pm 5\text{V}$ and $\pm 12\text{V}$) for computer logic circuits and peripherals. The dc-to-dc converter is typically designed with high frequency switching to reduce the size of passive components and to avoid the acoustic noise. Traditional designs have a switching frequency higher than 25 kHz.

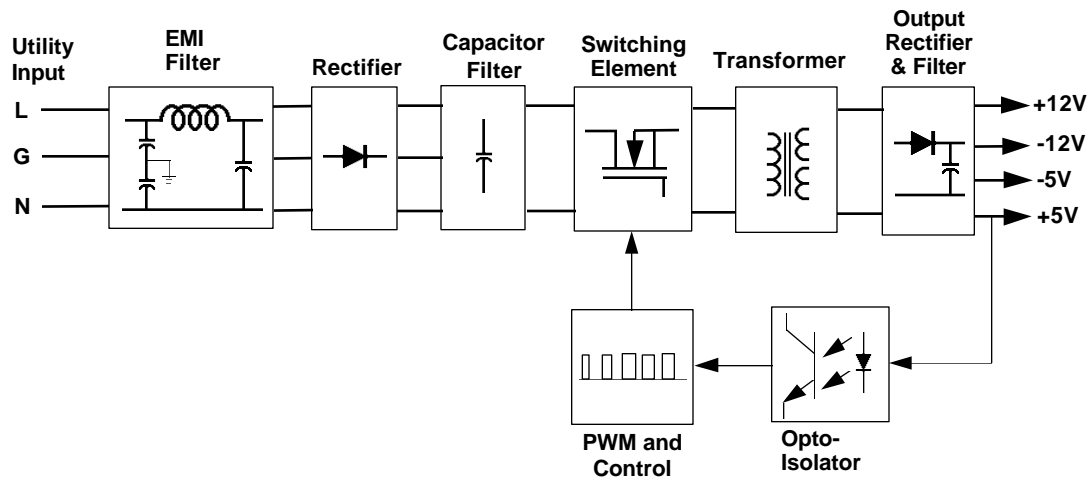


Figure B-1
Complete Block Diagram of a PC power supply

An optional ac interface circuit is to add a boost converter between the rectifier and the capacitor to eliminate the harmonics produced by the capacitor charging. The dc-to-dc

converter has several other options. Following sections will describe their circuits and advantages and disadvantages.

B.2

Boost Converter with Power Factor Correction (Model G, H, & GG)

Any dc-to-dc converter technologies can be used for power factor correction. Adding a boost converter between the ac input rectifier and the dc link capacitor is one of the most effective ways of eliminating harmonics generated by the capacitor charging. The basic principle of a boost converter operation is to control the inductor current to track the voltage across the rectifier output which is the absolute value of the ac input voltage presenting 120Hz sinusoidal pulses. The magnitude of the inductor current is controlled by the load, and the phase is synchronous with the rectifier output voltage. The current reflecting back to the ac line is then a pure sinusoidal wave. This technique is commonly called “boost converter with power factor correction.” To be precise, the power factor correction is actually obtained from harmonic elimination but not the traditional way of adding capacitor bank for correcting lagging reactive current.

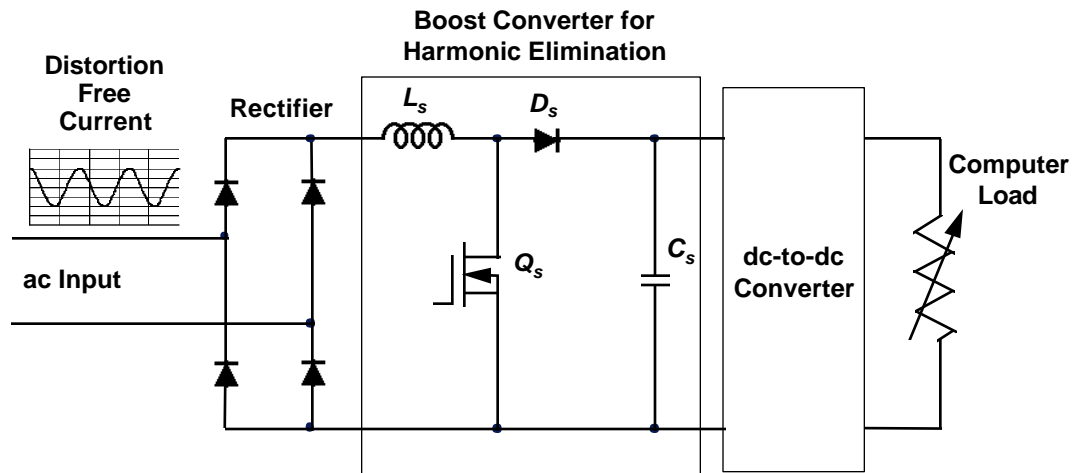


Figure B-2
Boost Converter for Harmonic Elimination and Power Factor Correction

The major advantage of using the boost converter for power factor correction is to allow the converter operating at a wide ac input voltage and frequency range. There is no need for the selecting switch to obtain a constant dc link voltage because the dc link voltage is now regulated by the boost converter switch, Q_s . Turning on Q_s will store the energy in the boost inductor, L_s . Turning off Q_s will release the energy through diode D_s to the storage capacitor, C_s . The voltage across C_s must be higher than the peak ac voltage. The control circuit in the power factor correction boost converter normally consists of two control loops, one for dc link voltage regulation and the other for phase tracking. Several controller ICs are already available for power factor correction boost converters.

B.3

Forward Converters

There are several versions of forward converters. If the transformer turns ratio is 1:1, the output voltage of the forward converter is always less than the input voltage and is directly proportional to the product of the input voltage and the transistor duty cycle. The forward converter needs to reset the winding flux after turning off the transistor. Two traditional flux resetting schemes are shown in Figures B-3 and B-4. One is to use a resetting winding and the other one is to use a resistor-capacitor-diode (RCD) clamping circuit.

1. Forward Converter with a Resetting Winding

This scheme requires an expensive transformer that consists of an extra winding to reset the transformer flux. The reset winding restricts that the duty cycle be less than 50 percent, lowering the utilization of the transformer. The advantages of this scheme are (1) low transistor voltage stress, (2) low transistor cost, (3) high efficiency, and (4) simple control.

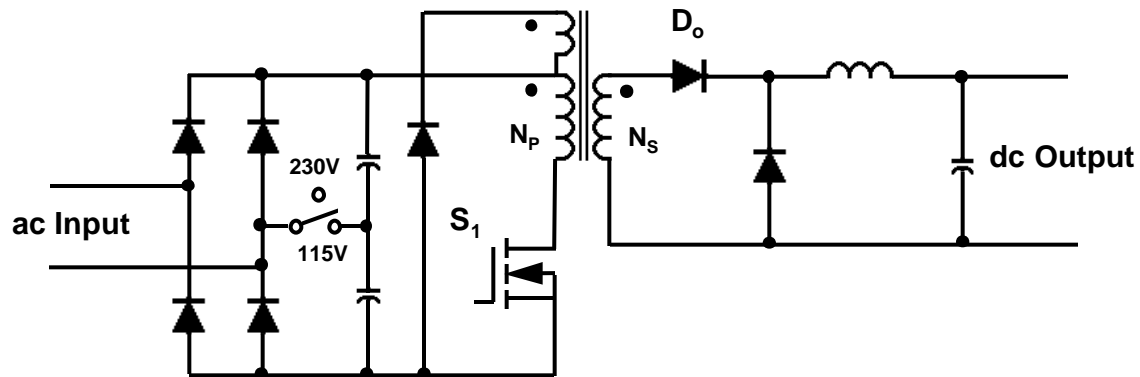


Figure B-3
Forward Converter with a Resetting Winding

2. Forward Converter with RCD Clamp (Model B & E)

This scheme was used in two models tested. One of them put the RCD network in the secondary winding. The operating principle has no difference between primary and secondary resetting schemes. Figure B-4 is a primary RCD resetting forward converter circuit. When the transistor S_1 turns on, a current along with its associated flux is built up in the primary winding. When the transistor S_1 turns off, the voltage across the transistor quickly swings up to higher than twice the supply voltage. The lossy RCD circuit is then conducting to reset the transformer flux and drop the voltage to the input voltage level

before the next switching cycle. Figure B-5 illustrates the switching waveform of a tested model. Voltage V_{ds} is the drain-to-source of the power MOSFET. The dc bus voltage, V_{dcs} , is about 320V, and the peak V_{ds} is about 580V.

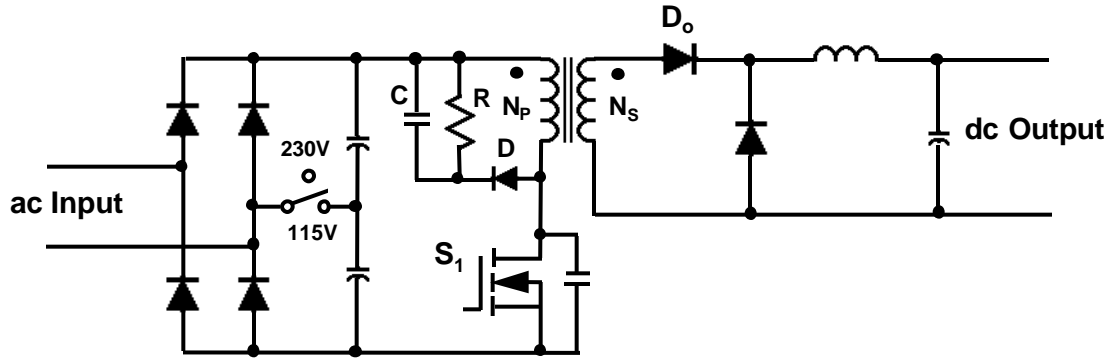


Figure B-4
Forward Converter with an RCD Clamp Circuit

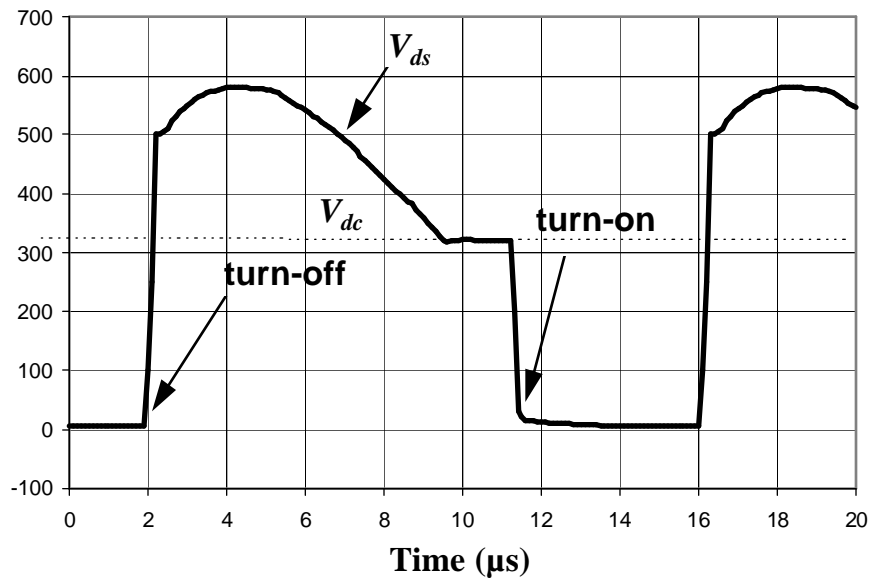


Figure B-5
Device Switching Waveform of the Forward Converter with RCD Clamp at 100-W output

The advantages of the RCD clamp type forward converter are its simple resetting scheme and low cost implementation. However, the high device voltage stress would need high voltage power MOSFET as the switching device which incurs more conduction loss. The lossy RCD circuit further reduces the power conversion efficiency.

3 Forward Converter with Active Clamp

It is possible to reduce the voltage stress by an active clamp circuit, shown in Figure B-5. An auxiliary switch S_c is added in the clamping circuit that turns on after the main device S_1 is turned off and its antiparalleled diode is conducting so that the auxiliary switch is turned on at zero-voltage. The voltage stress in this scheme can be limited to below 450V, about 150V lower than that in the RCD clamp scheme. A lower voltage rated switching device can be used to reduce the conduction loss. Overall, the efficiency can be improved by 3 to 5 percent. The problem of using this scheme is the additional auxiliary switch and its associated cost penalty. It is recommended that this circuit be developed for future power supplies.

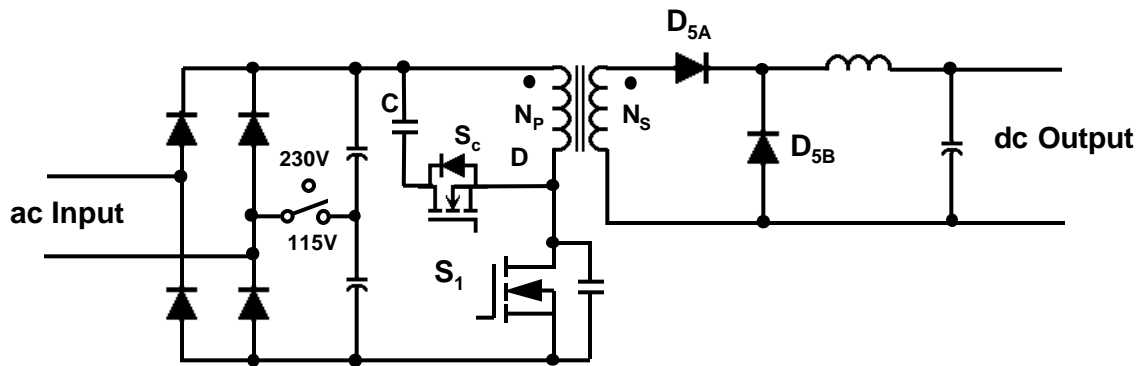


Figure B-5
Forward Converter with an Active Clamp Circuit

B.4

Half Bridge Converter (Model A, C, D, & F)

The half-bridge converter is a natural selection for the computer power supplies because it takes the advantage of the given capacitor center tap from the dual voltage rectifier-capacitor charging circuit. To avoid transformer saturation due to possible voltage unbalance, this type of converter normally connects a series capacitor between the input supply and the transformer. This capacitor needs to conduct the full current and provide near zero impedance for the switching frequency, typically requiring a large-size polypropylene capacitor. The advantages of this circuit topology are high efficiency, good utilization of transformer, and smaller output choke. The disadvantages are high cost due to additional transistor, isolation required for the high-side transistor, and large blocking capacitor.

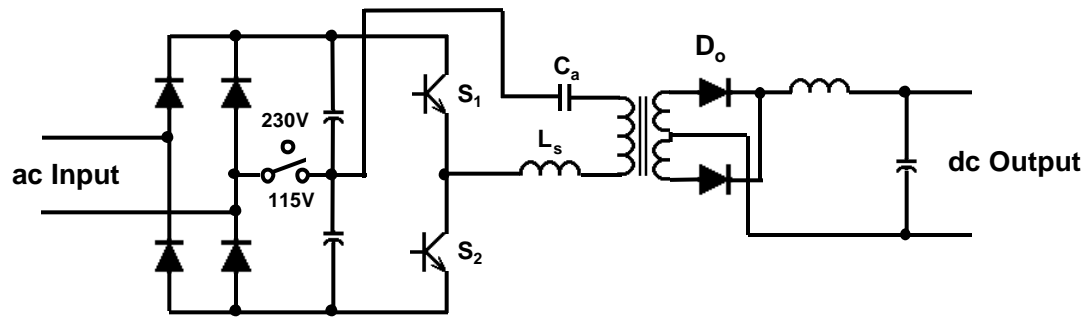


Figure B-6
Half Bridge Converter Circuit